INSTRUCTION MANUAL

PHASE TRAK 90 SERIES CARTRIDGE MACHINES

October, 1992 IM No. 597-9000

BROADCAST ELECTRONICS, INC.

IMPORTANT INFORMATION

EQUIPMENT LOST OR DAMAGED IN TRANSIT

When delivering the equipment to you, the truck driver or carrier's agent will present a receipt for your signature. Do not sign it until you have (a) inspected the containers for visible signs of damage and (b) counted the containers and compared with the amount shown on the shipping papers. If a shortage or evidence of damage is noted, insist that notation to that effect be made on the shipping papers before you sign them.

Further, after receiving the equipment, unpack it and inspect thoroughly for concealed damage. If concealed damage is discovered, immediately notify the carrier, confirming the notification in writing, and secure an inspection report. This item should be unpacked and inspected for damage WITHIN 15 DAYS after receipt. Claims for loss or damage will not be honored without proper notification of inspection by the carrier.

TECHNICAL ASSISTANCE AND REPAIR SERVICE

Technical assistance is available from Broadcast Electronics by letter or prepaid telephone or telegram. Equipment requiring repair or overhaul should be sent by common carrier, prepaid, insured and well protected. Do not mail equipment. We can assume no liability for inbound damage, and necessary repairs become the obligation of the shipper. Prior arrangement is necessary. Contact Customer Service Department for a Return Authorization.

FOR TECHNICAL ASSISTANCE

Phone (217) 224-9617 Customer Service

WARRANTY ADJUSTMENT

Broadcast Electronics, Inc. warranty is included in the Terms and Conditions of Sale. In the event of a warranty claim, replacement or repair parts will be supplied F.O.B. factory. At the discretion of Broadcast Electronics, the customer may be required to return the defective part or equipment to Broadcast Electronics, Inc. F.O.B. Quincy, Illinois. Warranty replacements of defective merchandise will be billed to your account. This billing will be cleared by a credit issued upon return of the defective item.

RETURN, REPAIR AND EXCHANGES

Do not return any merchandise without our written approval and Return Authorization. We will provide special shipping instructions and a code number that will assure proper handling and prompt issuance of credit. Please furnish complete details as to circumstances and reasons when requesting return of merchandise. All returned merchandise must be sent freight prepaid and properly insured by the customer.

REPLACEMENT PARTS

Replacement and Warranty Parts may be ordered from the address below. Be sure to include equipment model and serial number and part description and part number.

Broadcast Electronics, Inc.
4100 N. 24th St., P.O. Box 3606
Quincy, Illinois 62305
Tel: (217) 224-9600
Telex: 25-0142
Fax: (217) 224-9607

PROPRIETARY NOTICE

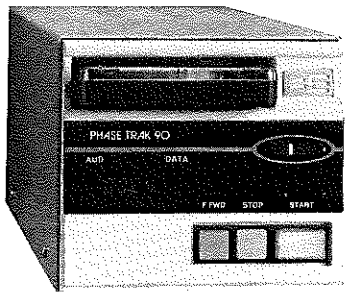
MODIFICATIONS

Broadcast Electronics, Inc. reserves the right to modify the design and specifications of the equipment in this manual without notice. Any modifications shall not adversely affect performance of the equipment so modified.

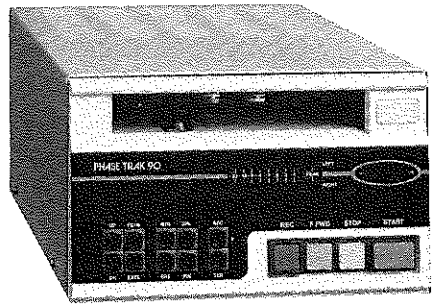
TECHNICAL MANUAL

BROADCAST ELECTRONICS
PHASE TRAK 90 SERIES
TAPE CARTRIDGE MACHINES
597-9000

TECHNICAL MANUAL
BROADCAST ELECTRONICS, INC.
PHASE TRAK 90 SERIES
CARTRIDGE MACHINES



PT-90 PLAYBACK



PT-90 RECORD/PLAYBACK

MODEL	PART NUMBER	DESCRIPTION
PT90P	900–9000–000	Single–Deck Monophonic Playback Cartridge Machine. NAB A or AA Cartridge Operation, 117V ac 50/60 Hz Power Supply.
PT90P	900–9000–300	Single–Deck Monophonic Playback Cartridge Machine. NAB A or AA Cartridge Operation, 220V ac 50/60 Hz Power Supply.
PT90PS	900–9002–000	Single–Deck Stereophonic Playback Cartridge Machine. NAB A or AA Cartridge Operation, 117V ac 50/60 Hz Power Supply.
PT90PS	900–9002–300	Single–Deck Stereophonic Playback Cartridge Machine. NAB A or AA Cartridge Operation, 220V ac 50/60 Hz Power Supply.
PT90RPS	900–9003–000	Single–Deck Stereophonic Record/Playback Cartridge Machine. NAB A, AA, B, and BB Cartridge Operation, 117V ac 50/60 Hz Power Supply.
PT90RPS	900–9003–300	Single–Deck Stereophonic Record/Playback Cartridge Machine. NAB A, AA, B, and BB Cartridge Operation, 220V ac 50/60 Hz Power Supply.

PT–90 PLAYBACK OPTIONAL ASSEMBLIES

——	900–9016	Tape Time Display, Factory Installed. Includes Front–Panel Four Digit LED Display and the Associated Digital Timer Circuitry.
——	250–0020	Maxtrax ® Stereo Playback Head, Factory Installed.

Maxtrax ® is a registered trademark of Pacific Recorders.

This equipment is a Class A (or Class B) digital apparatus which complies with the Radio Interference Regulation, CRC c.1374.

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SECTION I
GENERAL INFORMATION

1–1. INTRODUCTION.

1–2. Information presented by this section provides a general description of the Broadcast Electronics PT–90 series cartridge machines and lists equipment specifications.

1–3. EQUIPMENT DESCRIPTION.

1–4. The Broadcast Electronics PT–90 series cartridge machines are totally solid–state single deck playback and record/playback units designed for continuous on–air broadcast use. The PT–90 series includes monophonic and stereophonic playback units and a stereophonic record/play unit. Playback units are designed to accept NAB A or AA size cartridges. Record/playback units accept NAB A, AA, B, or BB size cartridges. A wide range of accessory products provide the flexibility required for any type of installation.

1–5. ELECTRICAL DESCRIPTION.

1–6. All PT–90 series cartridge machines are equipped with a brushless crystal controlled dc servo motor assembly which exhibits high reliability, low wow and flutter, and precise tape movement. Additional features include: 1) modular construction, 2) a precision–manufactured deck and PHASE–LOK V head assembly, 3) automatic/manual fast forward, 4) start lock–out operation, 5) cartridge–not–cued indications, 6) automatic elevated level cartridge sensing, and 7) DYNAFEX® noise reduction circuitry. Primary, secondary, tertiary, and FSK detection circuitry is standard on all models. Stereophonic playback and record/playback units are equipped with automatic non–encoding phase correction circuitry for precise audio reproduction.

1–7. **PHASE CORRECTION CIRCUITRY.** The automatic non–encoding phase correction circuitry is implemented on three hybrid circuits located on a plug–in audio playback module. The circuits monitor and correct the phase relationship between the left channel playback audio signal and the right channel playback audio signal to generate a precise in–phase stereophonic signal. Non–encoding phase correction allows the processing of stereophonic cartridges originally recorded on any cartridge machine. The phase correction circuit includes a front–panel moving bar LED display which provides a visual indication of the relative phase correction.

1–8. **FAST FORWARD CIRCUITRY.** An automatic/manual fast forward feature is incorporated into the control logic design for rapid recuing of tape cartridges. A programmable jumper on the logic module enables or disables the automatic fast forward feature. Manual fast forward operation is controlled by a front–panel switch/indicator.

1–9. **ELEVATED LEVEL SENSING CIRCUITRY.** The automatic elevated level sensing circuitry consists of a reflective sensor on the cartridge deck and a switching circuit on the audio module. When an elevated level cartridge (recorded at 250 nW/m) with special reflective tape is inserted into the deck, the gain of the audio circuitry will be automatically reduced by approximately 4 dB to provide normal output operating levels.

1–10. **NOISE REDUCTION CIRCUITRY.** The PT–90 audio circuitry features a DYNAFEX® noise reduction system to enhance the quality of the reproduced audio. The noise reduction circuit improves the signal–to–noise ratio by approximately 20 dB.

DYNAFEX® is a registered trademark of Circuit Research Labs.

1–11. **CUE CHANNEL DECODING CIRCUITRY.** The cue channel decoding circuitry is equipped with primary, secondary, and tertiary cue tone detectors. A precision FSK (3.5 kHz) decoder is also incorporated into the circuit design. This circuit generates an RS–232 serial data output for cartridge logging applications.

1–12. **RECORD CIRCUITRY.** The PT–90 record/playback unit is designed for complete record service. All record/playback unit record operations are directed by an Intel 80C39 microprocessor. The microprocessor provides the operator with a variety of record features. Record operating features include: 1) normal, learn, and manual program record functions, and 2) primary, secondary, and tertiary cue record functions.

1–13. Optimum operating convenience is provided by the learn mode. The learn mode automatically evaluates cartridge tape parameters and configures the unit for optimum record performance. The record parameters are stored in non–volatile memory and are accessed by the normal mode for future record operations. The unit may be manually configured for the desired record performance by manual mode operation.

1–14. The PT–90 record/playback unit also contains left and right channel LED VU meter displays. Cue channel erase operations are accomplished by an erase function. A built–in splice detector allows the operator to conveniently locate the tape splice for record operations. An FSK encoding circuit is incorporated into the record design for cartridge logging applications. A built–in test oscillator is provided for troubleshooting and record alignment procedures.

1–15. MECHANICAL DESCRIPTION.

1–16. All PT–90 series cartridge machines are completely modular in design for optimum service convenience. The power supply, control logic, playback audio circuitry, and record audio circuitry is implemented on plug–in modules which are accessible from the rear of the unit. Each unit is equipped with a precision–manufactured cartridge deck assembly and a direct drive dc servo motor assembly.

1–17. **DECK ASSEMBLY.** The PT–90 series cartridge machine deck is equipped with a cartridge guidance system, an air–damped solenoid, and the Broadcast Electronics PHASE LOK V head assembly. The cartridge guidance system is designed with spring–loaded components to channel a cartridge into the proper play position. An air–damped solenoid provides a rapid response to start commands. The PHASE LOK V head assembly provides the tape heads with a secure and stable environment. The head assembly is designed to permit independent adjustment of the head height/zenith and head azimuth.

1–18. **MOTOR ASSEMBLY.** The PT–90 series cartridge machines also features a direct–drive dc servo motor for precise tape movement. The motor is mounted to the half–inch thick rigid aluminum deck for maximum stability.

1–19. OPTIONS AND ACCESSORIES.

1–20. Refer to Table 1–1 for options and accessories available for the PT–90 series cartridge machines.

1–21. EQUIPMENT SPECIFICATIONS.

1–22. Refer to Table 1–2 for the electrical, mechanical, physical, and environmental specifications of the Broadcast Electronics PT–90 series cartridge machines.

DYNAFEX® is a registered trademark of Circuit Research Labs.

TABLE 1–1. PT–90 SERIES CARTRIDGE MACHINE OPTIONS AND ACCESSORIES
(Sheet 1 of 2)

OPTIONS AND ACCESSORIES	PART NUMBER
RECORDING EQUIPMENT	
MODEL 5409 MONOPHONIC RECORDER FOR THE PT–90 SERIES PLAYBACK CARTRIDGE MACHINE.	900–5409–011
Description: Model 5409 recorder provides monophonic record capabilities including primary, secondary, and tertiary cue tones for the model PT–90P cartridge machine.	
MODEL 5410 STEREOPHONIC RECORDER FOR THE PT–90 SERIES PLAYBACK CARTRIDGE MACHINE	900–5410–011
Description: Model 5410 recorder provides stereophonic record capabilities including primary, secondary, and tertiary cue tones for the model PT–90PS cartridge machine.	
INTERFACE CABLE KIT FOR PT–90P/PS CARTRIDGE MACHINES TO 5409/5410 RECORDERS.	970–0087
RECORD HEAD CONNECTOR KIT FOR PT–90P/PS WHEN INTERFACED WITH 5409/5410 RECORDERS.	970–0088
TELEPHONE ANSWERING EQUIPMENT	
MODEL PC–1 TELEPHONE INTERFACE.	900–0010
Description: The PC–1 telephone interface provides cartridge machine/telephone network communication. The unit answers incoming telephone calls and enables a cartridge machine for the purpose of transmitting a prerecorded message.	
RACK MOUNTING ACCESSORIES	
RACK MOUNT SHELF FOR EIA 19 INCH RACK, 7 INCH HEIGHT.	900–9013
1/3 RACK FILLER PANEL FOR 7 INCH RACK SHELF.	900–9014
1/2 RACK FILLER PANEL FOR 7 INCH RACK SHELF.	900–9015
1/6 RACK FILLER PANEL FOR 7 INCH RACK SHELF.	900–9017
SPARE PARTS KITS	
SPARE PARTS KIT FOR PT–90 PLAYBACK CARTRIDGE MACHINES.	970–0094
SPARE PARTS KIT FOR PT–90 RECORD/PLAYBACK CARTRIDGE MACHINES.	970–0114
TAPE SENSOR FOIL KIT (100 Qty.)	970–0099

TABLE 1–1. PT–90 SERIES CARTRIDGE MACHINE OPTIONS AND ACCESSORIES
(Sheet 2 of 2)

OPTIONS AND ACCESSORIES	PART NUMBER
TEST EQUIPMENT	
50–PIN EXTENDER CIRCUIT BOARD AND CABLE ASSEMBLY, PT–90 PLAYBACK OR RECORD/PLAYBACK UNITS.	950–0105
60–PIN EXTENDER CIRCUIT BOARD AND CABLE ASSEMBLY, PT–90 RECORD/PLAYBACK UNIT.	950–0106
TAPE HEAD AND TAPE GUIDE ALIGNMENT GAUGE KIT.	970–0102
MOTOR ALIGNMENT GAUGE KIT.	970–0103
CARTRIDGE MACHINE TEST TAPES:	
NAB Stereophonic Reproduce Alignment Tape, 160 nWb/m.	800–1005
NAB Monophonic Reproduce Alignment Tape, 160 nWb/m.	800–1005–001
NAB Cue Tone Calibration Cartridge	800–1095
Cut–Away Tape Alignment Test Cartridge	710–0132
ENCODING EQUIPMENT	
PT–90 DATA ENCODER SOFTWARE KIT	970–9000
Description: The data encoder software kit provides encoding capabilities with automatic features between the PT–90 cartridge machine and a personal computer.	
SPLICE–TRAK 90	900–9120
Description: The ST–90 provides high speed tape splice detection and tape erasing for A or AA sizes cartridges.	

TABLE 1–2. PT–90 SERIES CARTRIDGE MACHINE SPECIFICATIONS
(Sheet 1 of 2)

PARAMETER	SPECIFICATIONS
ELECTRICAL	
MOTOR	DC Servo.
TAPE SPEED	Programmable For 3.75 Inches/Second, 7.5 Inches/Second, or 15 Inches/Second, operation. Factory programmed at 7.5 Inches/Second.
TAPE SPEED ACCURACY	±0.2%.
TAPE TRANSPORT SYSTEM STOP TIME	80 msec Maximum at 7.5 Inches/Second Operation.
TAPE TRANSPORT SYSTEM START TIME	120 msec or less with Minimum Damping.
WOW AND FLUTTER	0.12% Maximum DIN. Referenced at 7.5 Inches/Second.
AUDIO OUTPUT IMPEDANCE	600 Ohms, Electronic Balanced, Floating.
AUDIO OUTPUT LEVEL	–20 dBm to +10 dBm, Continuously Variable. +24 dBm Clip Level.
AUDIO INPUT IMPEDANCE	Greater than 10 k Ohms, Balanced, Floating.
AUDIO INPUT LEVEL	–18 dBm to +20 dBm, Continuously Variable.
DISTORTION	
Record/Playback System	1.0% or Less Total–Harmonic–Distortion. Reference: 1 kHz at 250 nWb/m.
Reproduce Amplifier	0.5% or Less Total–Harmonic–Distortion.
NOISE (See Note)	
Hum and Noise	
Monophonic	
Noise Reduction Circuit Enabled	–80 dB. Reference: 1 kHz at 250 nWb/m.
Noise Reduction Circuit Disabled	–60 dB. Reference: 1 kHz at 250 nWb/m.
Stereophonic	
Noise Reduction Circuit Enabled	–80 dB. Reference: 1 kHz at 250 nWb/m.
Noise Reduction Circuit Disabled	–58 dB. Reference: 1 kHz at 250 nWb/m.
Squelch Noise (Noise Reduction Disabled)	–80 dB. Reference: 1 kHz at 250 nWb/m. Circuit
CROSSTALK	–50 dB or greater, Program Channel–to–Program Channel or Program Channel–to–Cue Channel at 1kHz.
FREQUENCY RESPONSE (See Note)	±2 dB, 40 Hz to 16 kHz.

NOTE: Specifications measured using 1975 NAB Standard Equalization.

TABLE 1–2. PT–90 SERIES CARTRIDGE MACHINE SPECIFICATIONS
(Sheet 2 of 2)

PARAMETER	SPECIFICATIONS
EQUALIZATION	
Standard	1975 NAB.
Optional	I.E.C., CCIR, 1965 NAB.
POWER REQUIREMENTS	
Standard	105V ac to 132V ac, 50/60 Hz.
Optional	210V ac to 264V ac, 50/60 Hz.
CUE TONES	1kHz (Primary), 150 Hz (Secondary), 8 kHz (Tertiary), and 3.5 kHz (FSK).
MECHANICAL	
NUMBER OF DECKS	One.
CARTRIDGE DECK SIZE	
Playback	A or AA Size Cartridges.
Record/Playback	A, AA, B, OR BB Size Cartridges.
TRANSPORT TYPE	Direct Drive Capstan.
PHYSICAL	
WEIGHT (Unpacked)	
Playback	21.5 Pounds (9.7 kg).
Record/Playback	27.5 Pounds (12.5 kg).
MOUNTING	
Standard	Desk–Top.
Optional	Rack Mount. 19 Inch (48.3 cm) EIA rack.
DIMENSIONS	
Playback	
Height	5.25 Inches (13.3 cm).
Width	5.875 Inches (14.9 cm).
Depth	16.5 Inches (41.9 cm).
Record/Playback	
Height	5.25 Inches (13.3 cm).
Width	8.75 Inches (22.2 cm).
Depth	16.5 Inches (41.9 cm).
ENVIRONMENTAL	
AMBIENT OPERATING TEMPERATURE	32°F to 122°F (0°C to 50°C).
HUMIDITY	95% Maximum. Non–Condensing.

SECTION II
INSTALLATION

2–1. INTRODUCTION.

2–2. This section contains the information required for the installation of the Broadcast Electronics PT–90 series cartridge machines.

2–3. UNPACKING.

2–4. The equipment becomes the property of the customer when the equipment is delivered to the carrier. Carefully unpack the cartridge machine. Perform a visual inspection to determine that no apparent damage has been incurred during shipment. All shipping materials should be retained until it is determined that the unit has not been damaged. Claims for damaged equipment must be promptly filed with the carrier or the carrier may not accept the claim.

2–5. The contents of the shipment should be as indicated on the packing list. If the contents are incomplete, or if the unit is damaged electrically or mechanically, notify both the carrier and Broadcast Electronics, Inc.

2–6. INSTALLATION.

2–7. PLACEMENT.

2–8. The standard PT–90 series cartridge machine is designed for desk–top placement. However, the unit may be installed in a 19 inch EIA rack assembly if desired. To provide adequate structural support, it is recommended that rack mounted units be installed in a PT–90 series rack shelf. Refer to illustration 597–9000–150 in SECTION VII for rack installation information. Install the cartridge machine by observing the following requirements and placing the unit in any convenient location.

A. Place the cartridge machine within reach of signal and power cables.

B. Do not place the cartridge machine near heat generating equipment.

C. To minimize noise, do not place the cartridge machine near equipment generating excessive 50 Hz or 60 Hz radiation.

D. For rack mounted cartridge machines, allow one inch of rack space above and below the unit for heat dissipation.

WARNING ***ENSURE NO PRIMARY POWER IS CONNECTED TO THE UNIT BEFORE PROCEEDING.***

WARNING

2–9. PT–90 CIRCUIT BOARD PROGRAMMING.

2–10. The PT–90 series cartridge machines are designed with a wide range of programmable operating characteristics to meet any installation requirement. The following text presents PT–90 control and operating parameters. Perform the circuit board programming and connection procedures as required for the desired operating or control parameter.

2–11. **MOTOR SPEED.** The cartridge machine motor speed is determined by circuitry on the motor control circuit board. The unit is shipped from the factory for 7.5 inches–per–second (IPS) operation. Playback units may be programmed for 3.75 IPS or 15 IPS operation. Record/playback units may be programmed for 3.75 IPS operation. Refer to Figures 2–1 and 2–2 to program the logic and motor control modules as required for the desired motor speed.

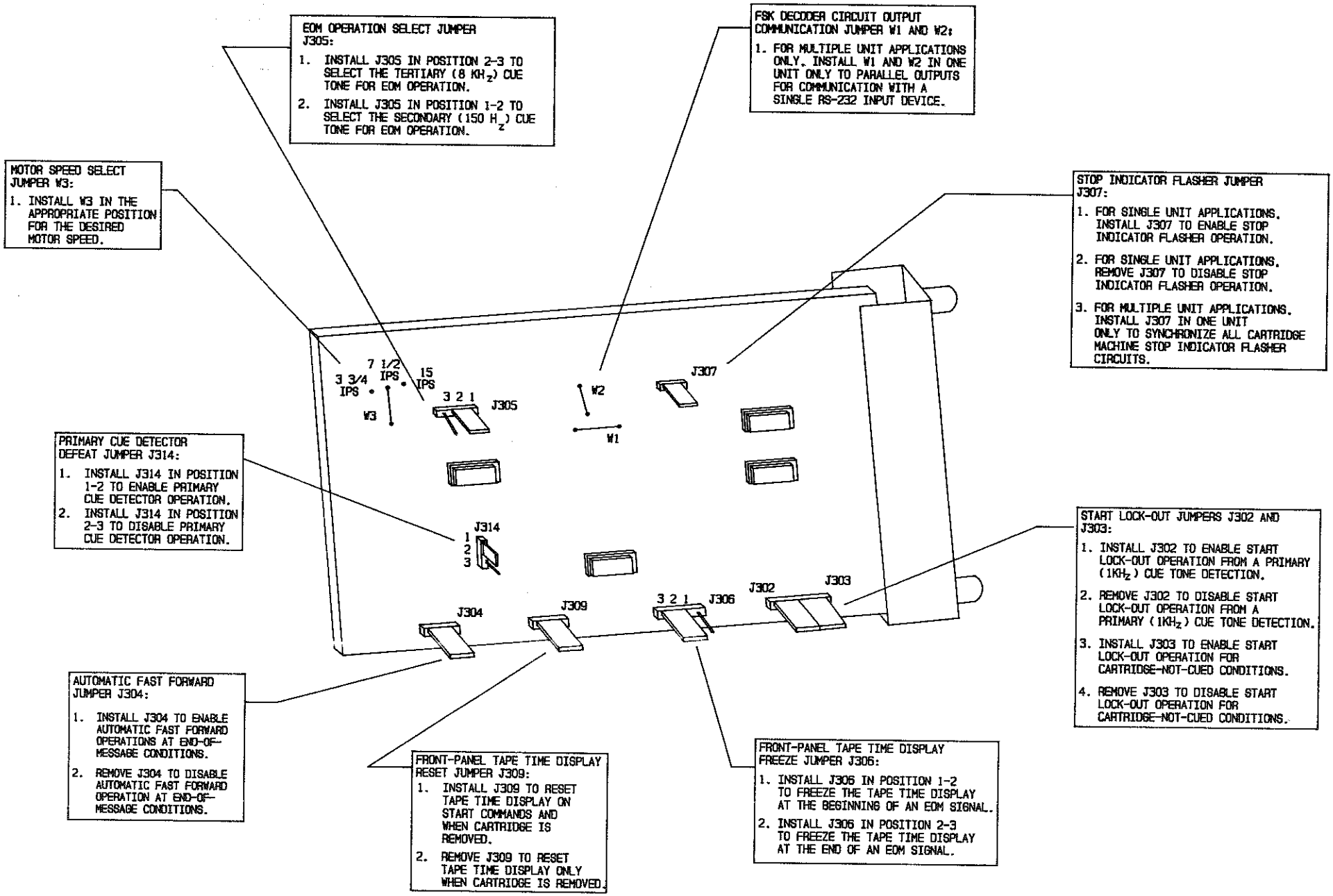

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FIGURE 2–1. PLAYBACK LOGIC MODULE JUMPER PROGRAMMING

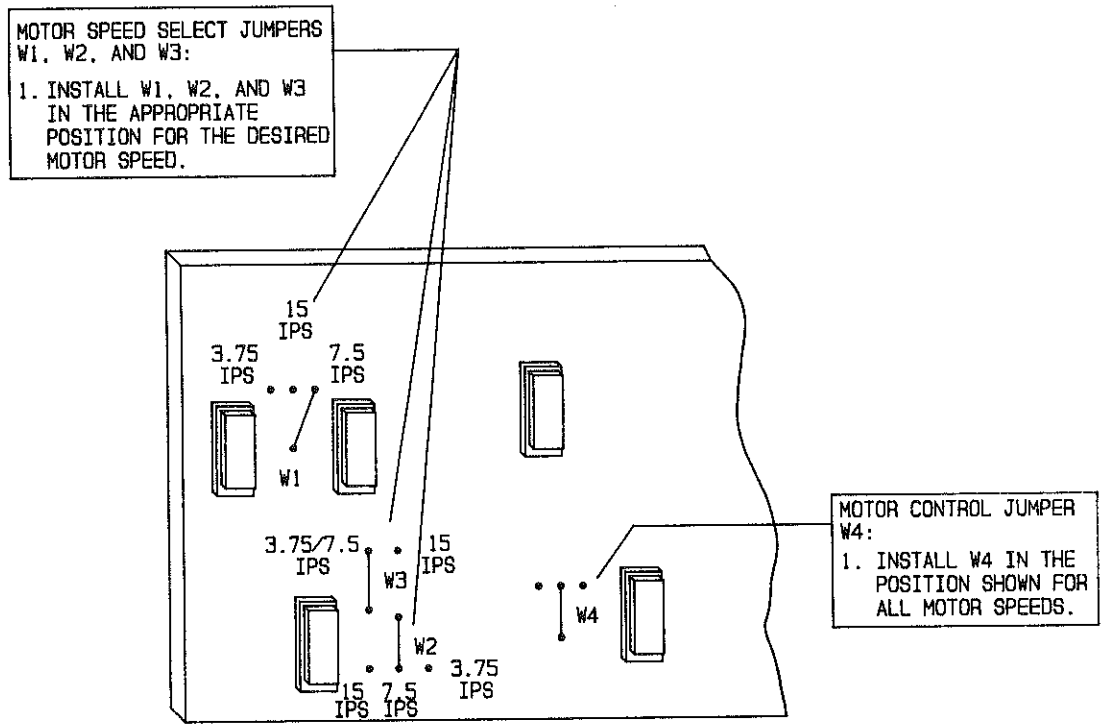

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FIGURE 2–2. MOTOR CONTROL CIRCUIT BOARD JUMPER PROGRAMMING

2–12. **END–OF–MESSAGE (EOM) CIRCUIT OPERATION.** The PT–90 control logic is designed to select either the secondary (150 Hz) or tertiary (8 kHz) cue tone for End–Of–Message (EOM) operation. The unit is shipped from the factory for 150 Hz EOM operation. Refer to Figure 2–1 to assign the desired cue tone for EOM operations.

2–13. **FREQUENCY–SHIFT–KEYING (FSK) DECODER OUTPUT COMMUNICATION.** An FSK decoder circuit is incorporated into the logic module design for cartridge data logging applications. The circuit is designed to interface with any RS–232 peripheral device (example: computer, terminal, or printer). The unit is shipped from the factory for single peripheral device communication in a single unit installation. For communication with a single peripheral device in multiple unit installations, refer to Figure 2–1 and program the logic module as required. Refer to Figure 2–6 for the FSK data output connections.

2–14. **START LOCK–OUT OPERATION.** A start lock–out circuit is provided to prevent duplicate on–air cartridge play. Start lock–out operation may be initiated from the termination of cartridge play by a primary (1 kHz) stop tone and/or by a cartridge–not–cued condition. The unit is shipped from the factory for start lock–out operation. Refer to Figure 2–1 and program the logic module for the desired application. Start lock–out conditions are indicated to the operator by the stop indicator flasher circuitry.

2–15. **STOP INDICATOR FLASHER OPERATION.** A circuit is provided to generate stop indicator flashing for two special operating conditions. The circuit will generate stop indicator flashing at a 1 Hz rate to indicate the termination of cartridge play by a primary (1 kHz) stop tone. The circuit will generate stop indicator flashing at a 2 Hz rate to indicate a cartridge–not–cued condition. The unit is shipped from the factory for stop indicator flasher operation. Refer to Figure 2–1 and program the logic module as required.

2–16. **Stop Indicator Flashing Synchronization.** For multiple unit installation, the stop indicator flashing may be synchronized. Stop indicator flashing may be synchronized by: 1) the appropriate circuit board programming and 2) the connection of a control line. Refer to Figure 2–1 and program the logic module as shown. Refer to Figure 2–6 and connect the control line to the units as shown. For synchronization operations, the master cartridge machine primary power (unit with the jumper installed) must be energized last to initialize the circuitry in each unit.

2–17. **FRONT–PANEL TAPE TIME DISPLAY OPERATION.** The tape time display control circuit may be programmed to freeze the time display at the beginning or the end of an EOM tone. The unit is shipped from the factory to freeze the tape time display at the end of an EOM tone. Refer to Figure 2–1 and program the logic module for the desired operating condition.

2–18. **FRONT–PANEL TAPE TIME DISPLAY RESET OPERATION.** The tape time display control circuit may be programmed to: 1) reset on start commands and when the cartridge is removed from the deck or 2) only when the cartridge is removed from the deck. The unit is shipped from the factory to reset on start commands and cartridge removal. Refer to Figure 2–1 and program the logic module for the desired operating condition.

2–19. **AUTOMATIC FAST FORWARD OPERATION.** Automatic fast forward operation may be initiated during EOM operations. The unit is shipped from the factory for automatic fast forward operation. Refer to Figure 2–1 and program the logic module as required for the desired operating condition.

2–20. **PRIMARY CUE TONE OPERATION.** The primary cue tone detector may be disabled if required to continuously reproduce program material. The unit is shipped from the factory for primary cue tone operation. Refer to Figure 2–1 and program the logic module as required for the desired operating condition.

2–21. **AUTOMATIC PHASE CORRECTION OPERATION.** The automatic phase correction circuitry may be disabled if required. The unit is shipped from the factory for phase correction operation. Refer to Figure 2–3 and enable or disable the automatic phase correction circuitry on the audio module as desired.

2–22. **NOISE REDUCTION SYSTEM OPERATION.** The noise reduction system may be disabled if required. The unit is shipped from the factory with the noise reduction system disabled. Refer to Figure 2–3 and enable or disable the noise reduction system on the audio module as desired.

2–23. **RECORD METER OPERATION.** PT–90 record/playback units are equipped with programmable record meter circuitry. The record meter may be configured to: 1) monitor the record input when the unit is operating in the record set mode and playback audio during the record mode or 2) monitor only record input audio during the record set or record modes. The unit is shipped from the factory with J207 installed. Refer to Figure 2–4 and program the record meter circuitry on the record bias module as required.

2–24. **AUDIO INTERFACING.**

2–25. The PT–90 series cartridge machines are equipped with XLR–type audio output receptacles on the audio module and record input receptacles on the record preamplifier module for convenient audio interfacing. Refer to the following information and connect the audio inputs and outputs to the unit as required.

2–26. **AUDIO OUTPUT CONNECTIONS.** XLR–type audio output connectors J405 and J406 on the audio module provide interfacing to external equipment (refer to Figure 2–5). XLR–type mating receptacles are supplied with the unit for interface cable construction (located in the accessory parts kit). Refer to Figure 2–5 and construct audio output interfacing cables using the mating receptacles and 2–conductor shielded audio cable such as Belden 8451 or equivalent.

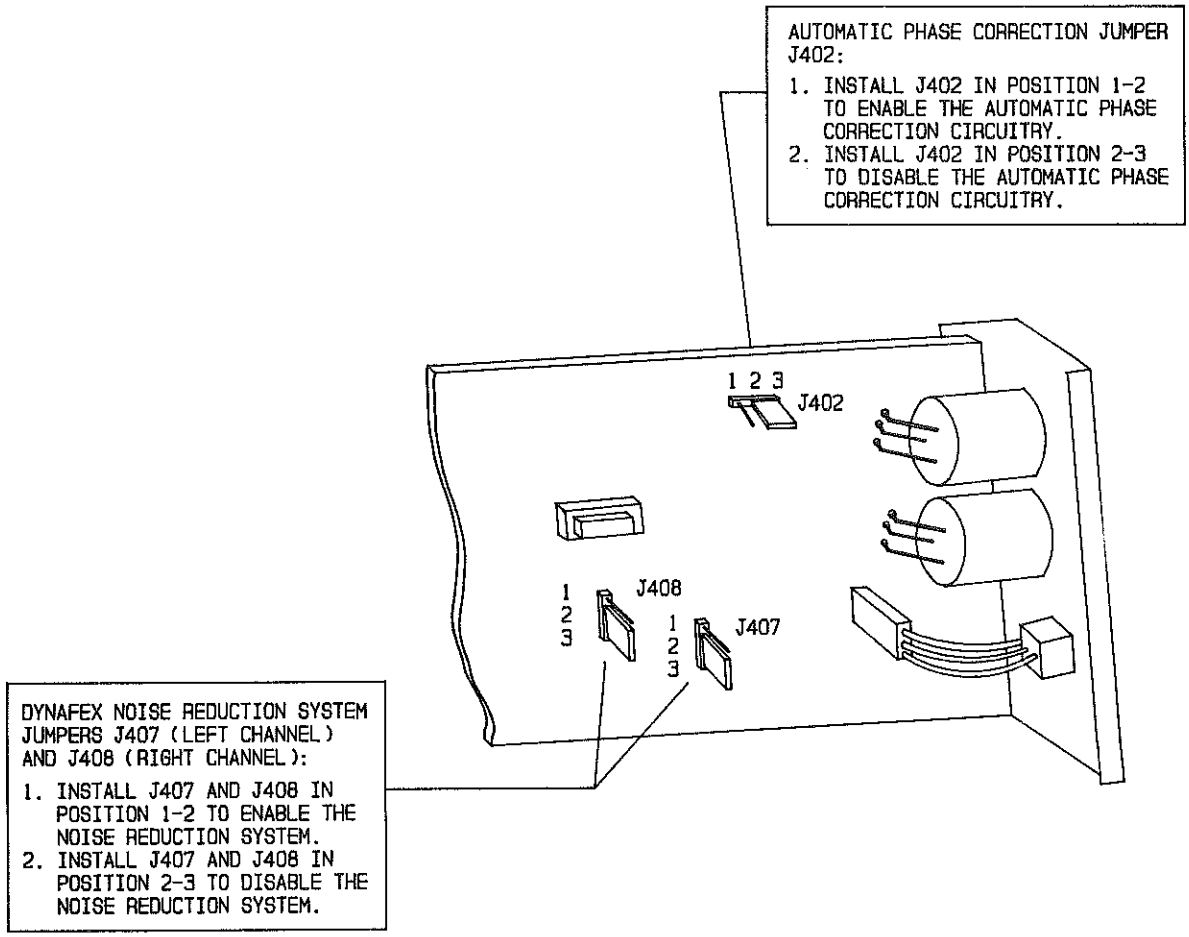

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FIGURE 2–3. AUDIO MODULE JUMPER PROGRAMMING

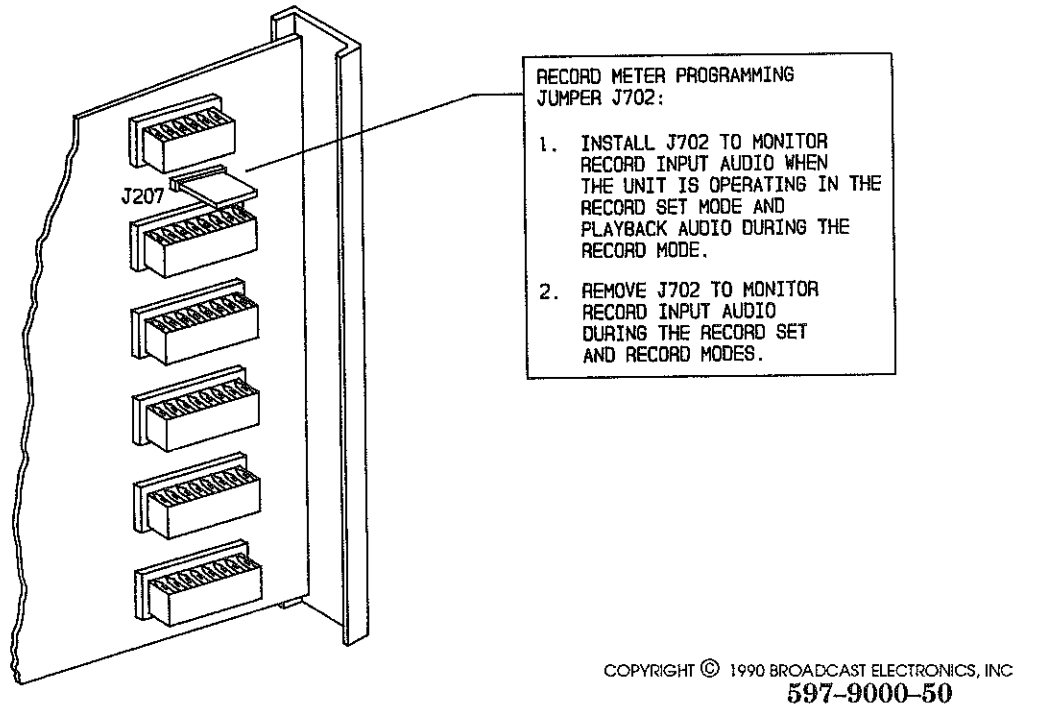

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FIGURE 2–4. RECORD BIAS MODULE JUMPER PROGRAMMING

2–27. **RECORD INPUT CONNECTIONS.** XLR–type record audio input connectors J902 and J903 on the record preamplifier module provide interfacing to external equipment (refer to Figure 2–5). XLR–type mating receptacles are supplied with the unit for interface cable construction (located in the accessory parts kit). Refer to Figure 2–5 and construct record audio input interfacing cables using the mating receptacles and 2–conductor shielded audio cable such as Belden 8451 or equivalent.

2–28. **REMOTE FUNCTIONS.**

2–29. The PT–90 series cartridge machines are equipped with playback and record remote control and status systems. Playback remote control and status interfacing is accessible at rear–panel remote connector J308 on the logic module. Record remote control and status interfacing is accessible at rear–panel remote connector J802 on the CPU module. Remote mating connectors are supplied with the unit for interface cable construction (located in the accessory parts kit).

2–30. **PLAYBACK REMOTE FUNCTIONS.** If playback remote functions are desired, refer to Figure 2–6 and the following text to connect remote control and status interfacing circuitry to receptacle J308 on the logic module as required.

2–31. **Start Operation And Indications.** Remote start control is accessible at J308 pin 1. A momentary contact to ground is required to initiate remote start operation. Remote start indications are available at J308 pin 3. The unit will output a LOW to indicate start operation. Attach the appropriate interface circuitry to connector J308 as required.

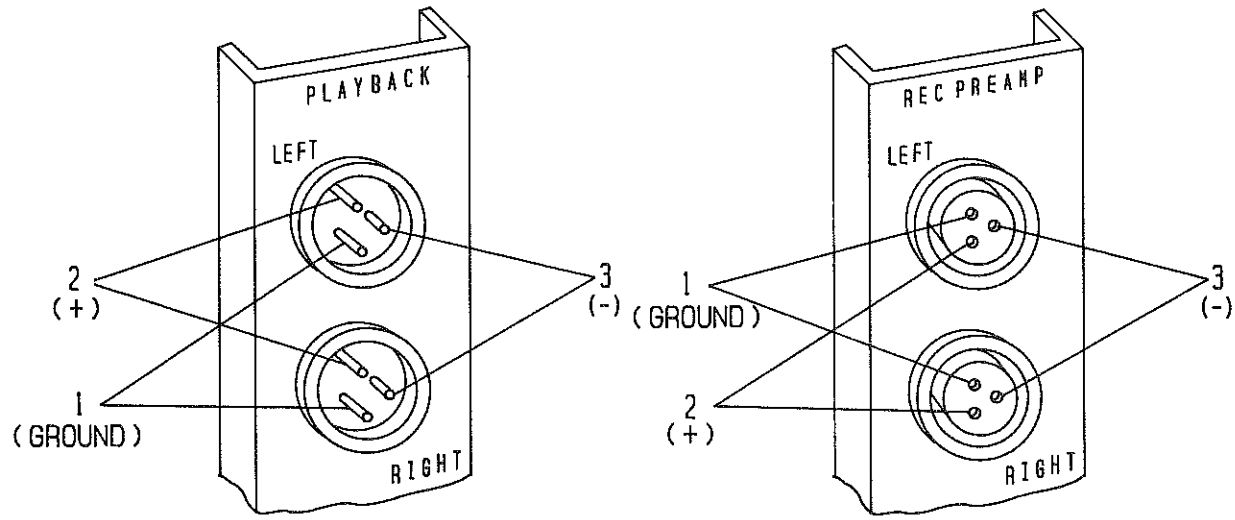

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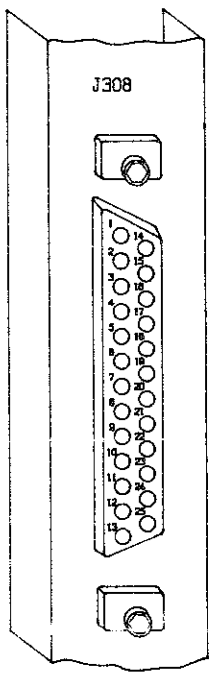
FIGURE 2–5. XLR CONNECTOR TERMINAL DESIGNATIONS



REMOTE CONNECTOR J308 PIN NO.	DESCRIPTION	CIRCUIT APPLICATION
1	START COMMAND	REMOTE CONTROL COMMANDS- MOMENTARY CONTACT TO GROUND REQUIRED TO ACTIVATE FUNCTION.
2	STOP COMMAND	
3	START INDICATOR	REMOTE STATUS INDICATORS- LOGIC 0 WHEN ACTIVE (+28V)
4	STOP INDICATOR	
5	AUDIO MUTE COMMAND	REMOTE CONTROL COMMAND- MOMENTARY CONTACT TO GROUND REQUIRED TO ACTIVATE FUNCTION.
6	VARISPEED MODE CONTROL	REMOTE VARISPEED MOTOR CONTROL CIRCUIT- CONTINUOUS CONTACT TO GROUND REQUIRED TO ACTIVATE FUNCTION. VARIES THE PROGRAMMED MOTOR SPEED A MINIMUM OF ±10%.
7	VARISPEED CONTROL FREQUENCY	ADJUSTABLE OSCILLATOR (9600 Hz NOMINAL)
8	STOP INDICATOR SYNCHRONIZATION CONTROL LINE	STOP INDICATOR SYNCHRONIZATION CONTROL LINE- FOR MULTIPLE UNIT APPLICATIONS, CONNECT ALL UNIT CONTROL LINES TOGETHER TO SYNCHRONIZE STOP INDICATOR FLASHING OPERATIONS. (REFER TO JUMPER PROGRAMMING FOR STOP INDICATOR FLASHING OPERATIONS)
9	SECONDARY CUE TONE INDICATOR	REMOTE STATUS INDICATORS- LOGIC 0 WHEN ACTIVE (+28V)
10	TERTIARY CUE TONE INDICATOR	
11	+28V dc SUPPLY	+28V dc SUPPLY
12	TERTIARY CUE TONE RELAY CONTACT	CUE TONE RELAY CONNECTIONS- 100V dc AT 0.5 AMPERES MAXIMUM
13	SECONDARY CUE TONE RELAY CONTACT	
14	POWER SUPPLY GROUND	POWER SUPPLY GROUND
15	FAST FORWARD COMMAND	REMOTE CONTROL COMMAND- MOMENTARY CONTACT TO GROUND REQUIRED TO ACTIVATE FUNCTION.
16	FAST FORWARD INDICATOR	REMOTE STATUS INDICATOR- LOGIC 0 WHEN ACTIVE (+28V)
17	AUXILIARY START PULSE OUTPUT	AUXILIARY START PULSE OUTPUT- A LOW ACTIVE PULSE FOR EXTERNAL START OPERATIONS.
18	POWER SUPPLY GROUND	7 SIGNAL GROUND
19	RS-232 DATA OUTPUT	3 RS-232 DATA INPUT
20	RS-232 CARRIER PRESENT	8 RS-232 CARRIER DETECT — RS-232 DATA CONNECTIONS; RS-232 INPUT DEVICE RECEPTACLE
21	RS-232 DATA INDICATOR	REMOTE STATUS INDICATOR- LOGIC 0 WHEN ACTIVE (+28V)
22	CUE AUDIO OUTPUT	CUE AUDIO OUTPUT CONNECTIONS
23	CUE AUDIO GROUND	
24	TERTIARY CUE TONE RELAY CONTACT	CUE TONE RELAY CONNECTIONS- 100V dc AT 0.5 AMPERES MAXIMIM
25	SECONDARY CUE TONE RELAY CONTACT	

FIGURE 2–6. REMOTE CONTROL RECEPTACLE CONNECTION

2–32. **Stop Operation And Indications.** Remote stop control is accessible at J308 pin 2. A momentary contact to ground is required to initiate remote stop operation. Remote stop indications are available at J308 pin 4. The unit will output a LOW to indicate the termination of deck operation. Attach the appropriate interface circuitry to connector J308 as required.

2–33. **Audio Mute Operation.** Remote audio muting is accessible at J308 pin 5. A momentary contact to ground is required to initiate the audio mute operation.

2–34. **Secondary Cue Tone Relay Contacts And Indications.** Secondary cue tone relay contacts are accessible at J308 pins 13 and 25 for control of external equipment. The relay contacts are rated for 100V dc at 0.5 amperes maximum. Remote secondary cue tone indications are available at J308 pin 9. The unit will output a LOW to indicate a secondary cue tone detection. Attach the appropriate interface circuitry to connector J308 as required.

2–35. **Tertiary Cue Tone Relay Contacts And Indications.** Tertiary cue tone relay contacts are accessible at J308 pins 12 and 24 for control of external equipment. The relay contacts are rated for 100V dc at 0.5 amperes maximum. Remote tertiary cue tone indications are available at J308 pin 10. The unit will output a LOW to indicate a tertiary cue tone detection. Attach the appropriate interface circuitry to connector J308 as required.

2–36. **Fast Forward Operation And Indications.** Remote fast forward control is accessible at remote connector J308 pin 15. A momentary contact to ground is required to initiate fast forward operation. Remote fast forward indications are available at J308 pin 16. The unit will output a LOW to indicate fast forward operation. Attach the appropriate interface circuitry to connector J308 as required.

2–37. **Vari–Speed Motor Operation.** The PT–90 series cartridge machines are equipped with a vari–speed feature which allows the operator to vary the cartridge machine motor speed a minimum of ±10%. An adjustable 9600 Hz reference is required at J308 pin 7 for motor control. Connect a LOW to J308 pin 6 to initiate vari–speed operation. When vari–speed operation is initiated and the motor reference is varied (example: 10%), the control circuitry will act to vary the programmed motor speed a corresponding amount (10%).

2–38. **Auxiliary Start Pulse Output.** An auxiliary start pulse is accessible at J308 pin 17 for control of external equipment. The unit will output a LOW for external start applications.

2–39. **Cue Audio Output.** Cue audio is accessible at J308 pins 22 and 23 for remote monitoring applications. Attach the appropriate interface circuitry to connector J308 as required.

2–40. **FSK Data Output Connections.** RS–232 data from cartridge FSK information is available at J308 pins 18, 19, and 20 for communication with an external peripheral device. The unit will output a LOW at J308 pin 21 to indicate FSK data detection. Attach the appropriate interface circuitry to connector J308 as required.

2–41. **RECORD REMOTE FUNCTIONS.** If record remote functions are desired, refer to Figure 2–7 and the following text to connect remote control and status interfacing circuitry to receptacle J802 on the CPU module as required.

2–42. **Record Control and Indications.** Remote record mode control is accessible at J802 pin 5. A momentary contact to ground is required to initiate remote record operation. Remote record indications are available at J802 pin 3. The unit will output a LOW to indicate record mode operation. Attach the appropriate interface circuitry to connector J802 as required.

2–43. **Primary, Secondary, and Tertiary Cue Tone Record Control.** Primary, secondary, and tertiary cue tone remote record control is accessible at remote connector J802. A momentary contact to ground is required to initiate each remote record operation. Attach the appropriate interface circuitry to connector J802 as required. The following list presents primary, secondary, and tertiary cue tone record control pin locations.

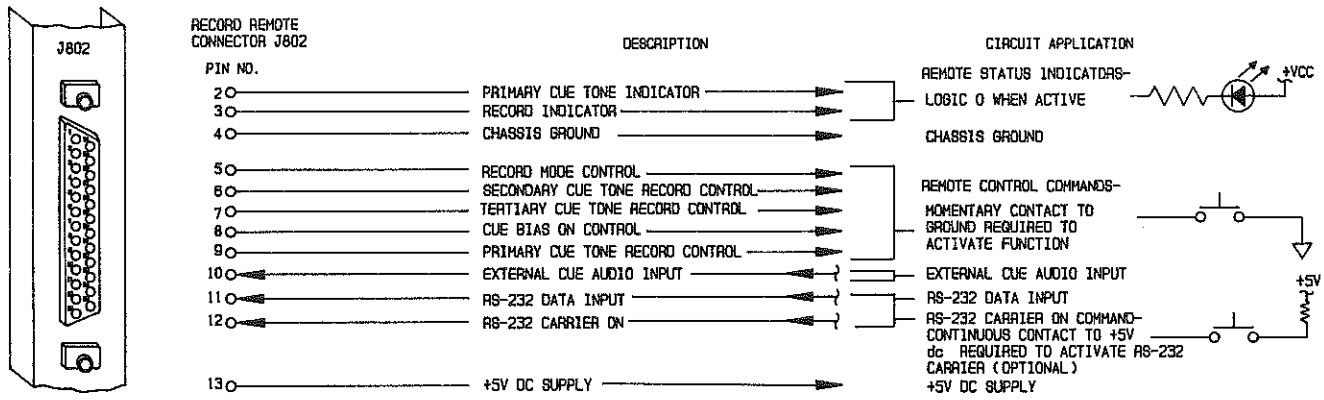


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FIGURE 2–7. RECORD REMOTE CONTROL RECEPTACLE CONNECTIONS

REMOTE CONNECTOR J802 PIN NO.	DESCRIPTION
6	Secondary Cue Tone Record Control
7	Tertiary Cue Tone Record Control
9	Primary Cue Tone Record Control

2–44. **Primary Cue Tone Record Status Indications.** Primary cue tone record status indications are available at J802 pin 2. The unit will output a LOW to indicate primary cue tone record operations. Attach the appropriate interface circuitry to connector J802 as required.

2–45. **External Cue Record.** An external cue tone record feature is incorporated into the remote control circuit design. The external cue record feature includes cue record control and a cue tone audio input. If external cue record operations are desired, connect a momentary contact to ground switch to the cue bias on terminal at J802 pin 8. Connect the external cue audio to J802 pin 10.

2–46. **FSK Data Encoding.** The PT–90 record/playback cartridge machines are designed for FSK data encoding operations. Figure 2–8 presents typical FSK data encoding applications. The FSK encoding system requires the use of a personal computer with text editing software or a data terminal with memory and block–transmit capabilities. The computer or data terminal must also be equipped with a serial output port.

2–47. The encoding system may be configured for manual or automatic modes of operation. A manual encoding system involves normal computer/data terminal operation and manual operation of the cartridge machine. The automatic encoding system requires the implementation of the Data Encoder Software Option which automates the computer/data terminal and cartridge machine operations. Refer to the following text to configure the data encoding system for the desired operation.

2–48. For automatic and manual FSK data encoding, refer to Figure 2–8 and connect the computer/data terminal serial port to the cartridge machine as shown. For manual encoding systems with the cartridge machine placed in a remote location, connect a remote start switch/indicator to the cartridge machine as shown.

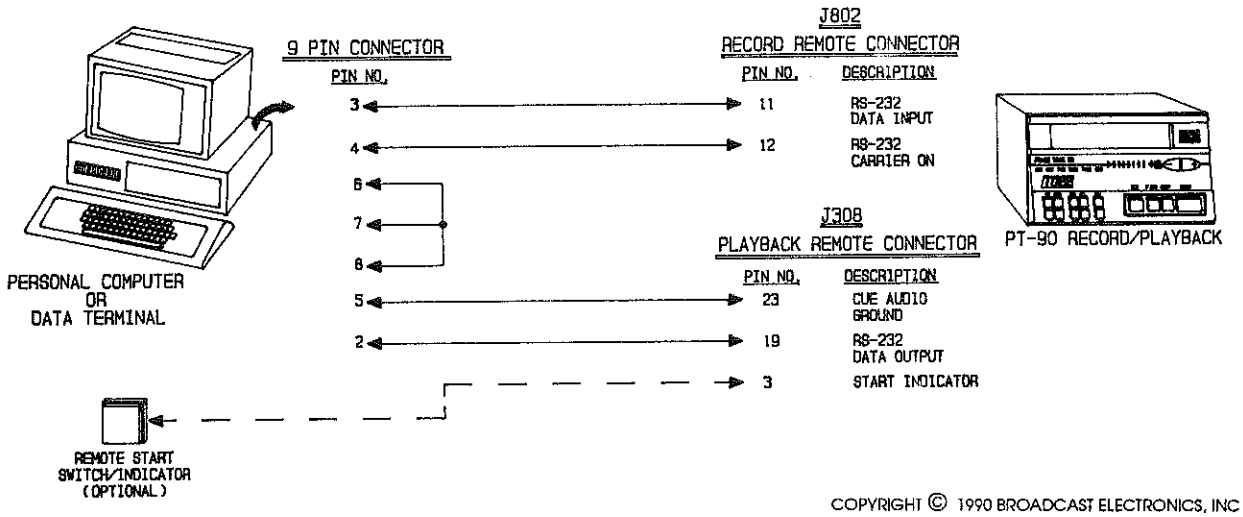

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FIGURE 2–8. FSK ENCODING APPLICATIONS

2–49. AUTOMATIC AUDIO MUTING.

2–50. An automatic audio muting feature is incorporated into the PT–90 series control circuit design. The feature will automatically mute associated cartridge machines without the operation of an audio switcher in multiple unit installations. Audio will be muted in all cartridge machines with the exception of the on–air unit. If automatic audio muting is desired, refer to Figure 2–9 and connect the units as shown.

2–51. AUTOMATIC START SEQUENCING.

2–52. All PT–90 series cartridge machines may be configured for automatic start sequencing. The following text presents wiring procedures for a typical start sequence. However, the sequence may be modified as required to achieve any start sequence.

2–53. **SEQUENCE.** Figure 2–10 presents wiring connections for a start sequence described in the following text. Refer to Figure 2–10 and connect the units as shown.

START SEQUENCE

A. Cartridge machine 1 will start cartridge machine 2.

B. Cartridge machine 2 will start cartridge machine 3.

C. Cartridge machine 3 will start cartridge machine 4.

D. Cartridge machine 4 will start cartridge machine 5.

E. Cartridge machine 5 will start cartridge machine 1.

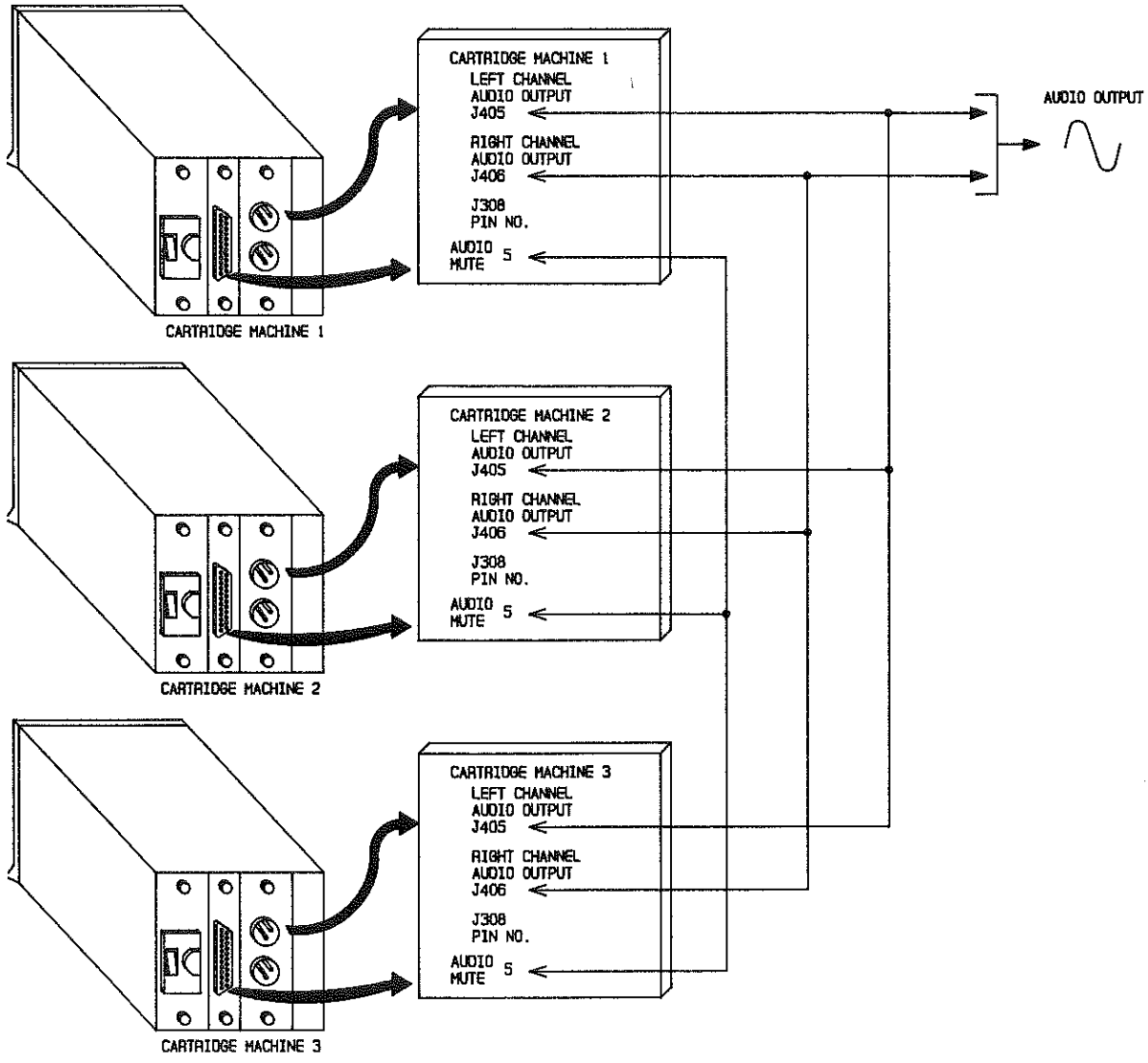

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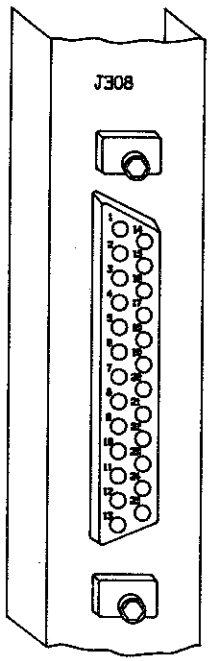
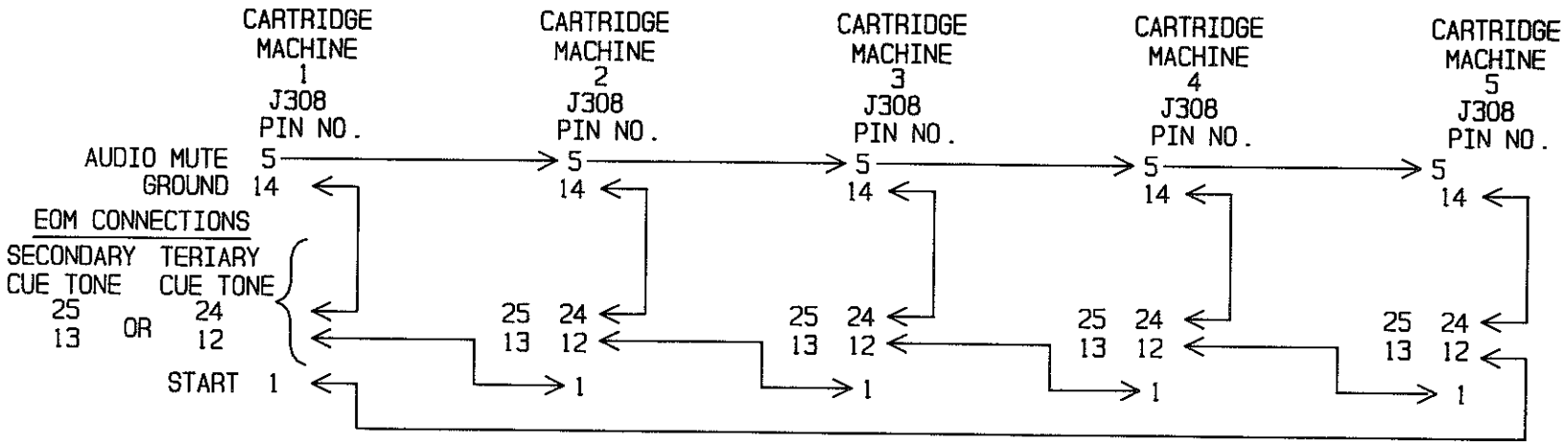
FIGURE 2-9. AUTOMATIC AUDIO MUTING





START SEQUENCE

1. CARTRIDGE MACHINE 1 WILL START CARTRIDGE MACHINE 2.
2. CARTRIDGE MACHINE 2 WILL START CARTRIDGE MACHINE 3.
3. CARTRIDGE MACHINE 3 WILL START CARTRIDGE MACHINE 4.
4. CARTRIDGE MACHINE 4 WILL START CARTRIDGE MACHINE 5.
5. CARTRIDGE MACHINE 5 WILL START CARTRIDGE MACHINE 1.

NOTE:

1. THE START SEQUENCE MAY BE MODIFIED TO ACHIEVE ANY START SEQUENCE REQUIREMENT.
2. FOR SECONDARY CUE TONE EOM ASSIGNMENTS, CONNECT JUMPERS TO PINS 25 AND 13. FOR TERTIARY CUE TONE EOM ASSIGNMENTS, CONNECT JUMPERS TO PINS 24 AND 12.

597-9000-110

FIGURE 2–10. PT-90 SERIES CARTRIDGE MACHINE START SEQUENCING

2–54. GROUND SYSTEM PROGRAMMING.

WARNING *DO NOT REMOVE THE JUMPER BETWEEN TERMINALS E3 AND E4 DURING GROUND SYSTEM PROGRAMMING.*

WARNING

2–55. The PT–90 is equipped with a programmable ground system. The system consists of a jumper network and two ground terminals located on the power supply module (refer to Figure 2–11). The jumper network and the ground terminals are designed to distribute and isolate ground circuits as required for optimum performance. The unit is shipped from the factory in a star ground configuration. If an alternate ground configuration is desired, refer to Figure 2–11 and program the system as required. Ensure the chassis ground circuit is connected to earth ground using a braided or solid copper conductor.

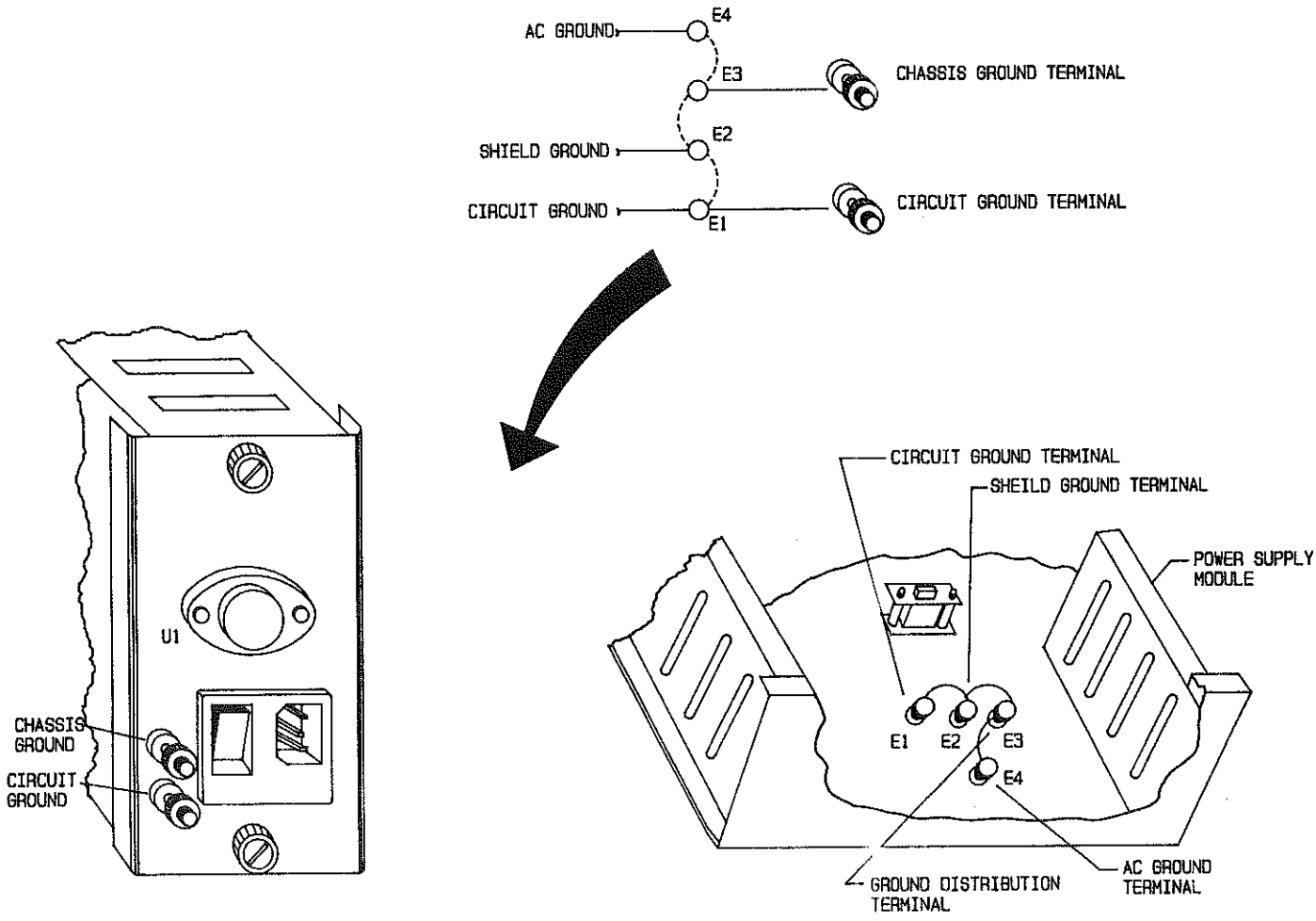


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FIGURE 2–11. PT–90 GROUND SYSTEM

2–56. When ground system programming is completed, an important consideration in assuring low noise performance from the cartridge machine is the grounding and shielding of the various audio interconnections. First, ensure the cartridge machine circuit ground and any required internal ground terminal is connected to an earth ground using a braided or solid copper conductor. Second, the shields from audio conductors must be grounded to prevent the coupling of extraneous noise. Generally, the shields are grounded at the studio audio console. However, the shields may require grounding at the cartridge machine or at a point between the cartridge machine and the studio audio console. Particular care must be exercised to avoid ground loops at patch panels, external switching equipment, uninsulated jacks on associated equipment, and grounded racks or cabinets.

2–57. **AC POWER CONNECTION.**

WARNING *ENSURE ALL PRIMARY POWER IS DISCONNECTED BEFORE PROCEEDING.*

WARNING

2–58. The PT–90 series cartridge machines are programmed for the proper power supply voltage when shipped from the factory. The operating voltage requirement for the unit is indicated on the cartridge machine identification plate which is located on the cartridge machine side–panel. If the unit is to be operated from an ac power source other than the original factory programmed source, re–program the unit by operating the 110V/220V power switch on the power supply module to the desired position (refer to Figure 2–12).

2–59. Remove the fuse from the rear–panel fuse–holder. For playback only units, ensure the fuse is a slow–blow type rated at 0.5A for 105V to 132V operation or 0.25A for 210V to 264V operation. For record/playback units, ensure the fuse is a slow–blow type rated at 1.0A for 105V to 132V operation or 0.5A for 210V to 264V operation.

2–60. Ensure the rear–panel power switch is operated to OFF and connect the cartridge machine line cord to the appropriate power source.

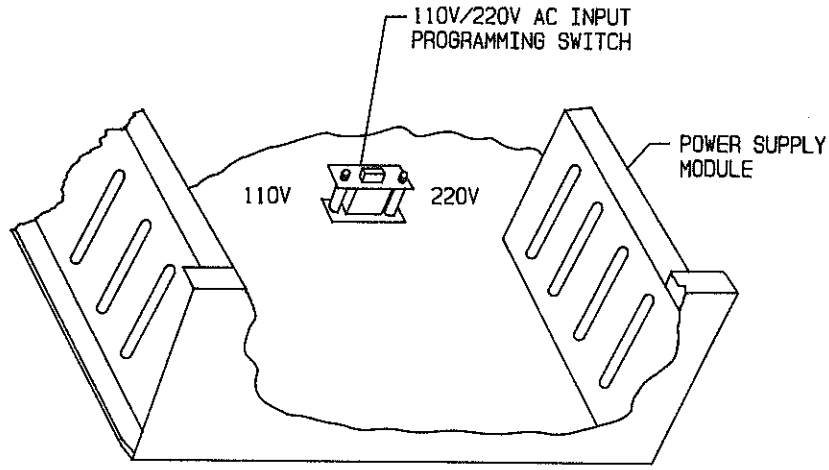

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FIGURE 2–12. 110V/220V PROGRAMMING SWITCH

2–61. **ELECTRICAL ADJUSTMENTS.**

2–62. **AUDIO OUTPUT LEVEL ADJUSTMENT.** The cartridge machine audio output level is factory adjusted to 0 dBm. If an alternate output level is required, refer to the ELECTRICAL ADJUSTMENTS procedures in SECTION V, MAINTENANCE and perform the OUTPUT LEVEL ADJUSTMENT procedure.

NOTE *FOR PROPER PHASE CORRECTION OPERATION, ALIGN THE PT–90 PLAYBACK AZIMUTH TO THE STATION IN–HOUSE CARTRIDGE STANDARD.*

NOTE

2–63. **HEAD AZIMUTH ADJUSTMENT.** For stereophonic cartridge machines, the cartridge machine playback azimuth must be aligned to the station in–house cartridge standard for proper phase correction operation. Refer to HEAD ADJUSTMENTS in SECTION V, MAINTENANCE and perform the **Playback Head Azimuth Adjustment Procedure** to align the cartridge machine playback azimuth to the station in–house standard.

2–64. **OPTIONAL EQUIPMENT INSTALLATION.**

2–65. **GENERAL.** The following list presents related publications which provide data required for the installation of options and accessories associated with the PT–90 series cartridge machines.

OPTION OR ACCESSORY	PUBLICATION NUMBER
Model 5409 or 5410 Recorder	597–0097–001
Model PC–1 Telephone Interface	597–0047

SECTION III
OPERATION

3–1. INTRODUCTION.

3–2. This section identifies all controls and indicators associated with the PT–90 series cartridge machines and provides standard operating procedures.

3–3. CONTROLS AND INDICATORS.

3–4. Refer to Figure 3–1 for the location of all controls and indicators associated with the unit. The function of each control or indicator is described in Table 3–1.

3–5. OPERATION.

NOTE *THE FOLLOWING PROCEDURE ASSUMES THAT THE CARTRIDGE MACHINE IS COMPLETELY INSTALLED AND IS FREE OF ANY DISCREPANCIES.*

NOTE

3–6. PLAYBACK OPERATION.

3–7. Operate the rear–panel power switch to ON.

3–8. Insert an NAB A or AA size tape cartridge into the deck on playback only units. Insert an NAB A, AA, B, or BB size tape cartridge into the deck on record/playback units. When the cartridge is inserted, the following events will occur:

A. The deck **STOP** switch/indicator will illuminate.

B. The tape time display will illuminate.

3–9. Depress the deck **START** switch/indicator to begin cartridge play operation. When the **START** switch/indicator is depressed, the following events will occur:

A. The deck **START** switch/indicator will illuminate.

B. The deck **STOP** switch/indicator will extinguish.

C. The **AUD** indicator will illuminate.

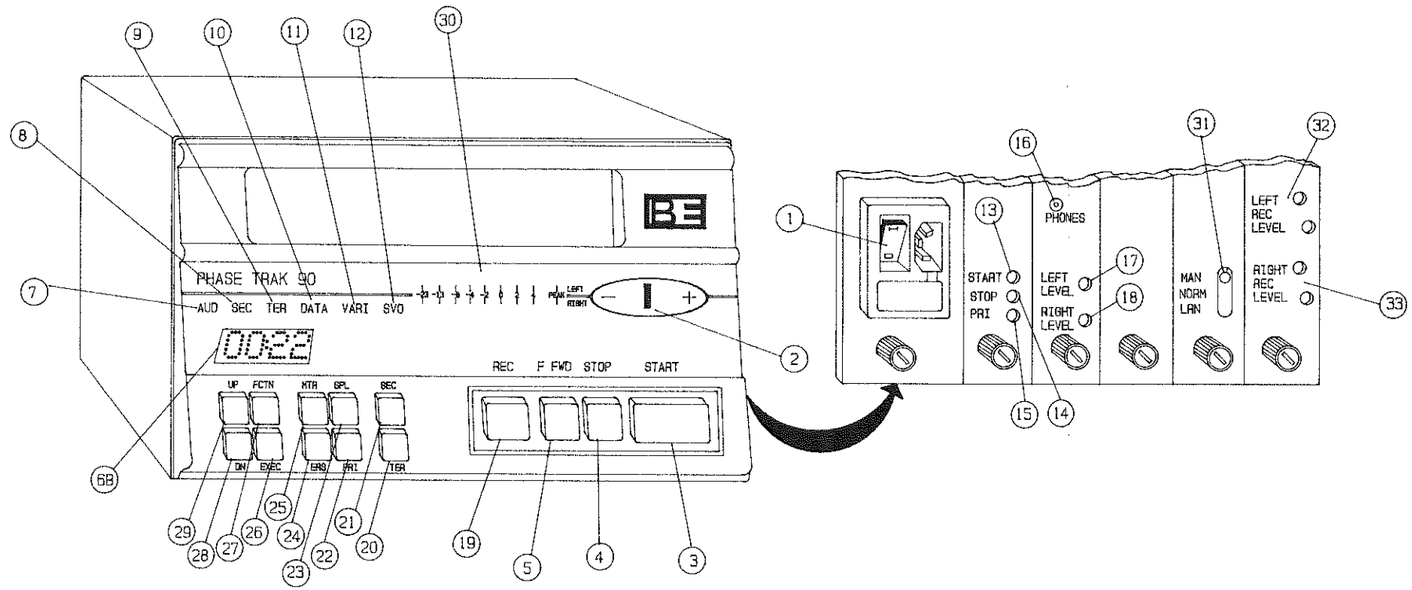
D The rear–panel **START** indicator will illuminate.

E. The tape time display will begin operation.

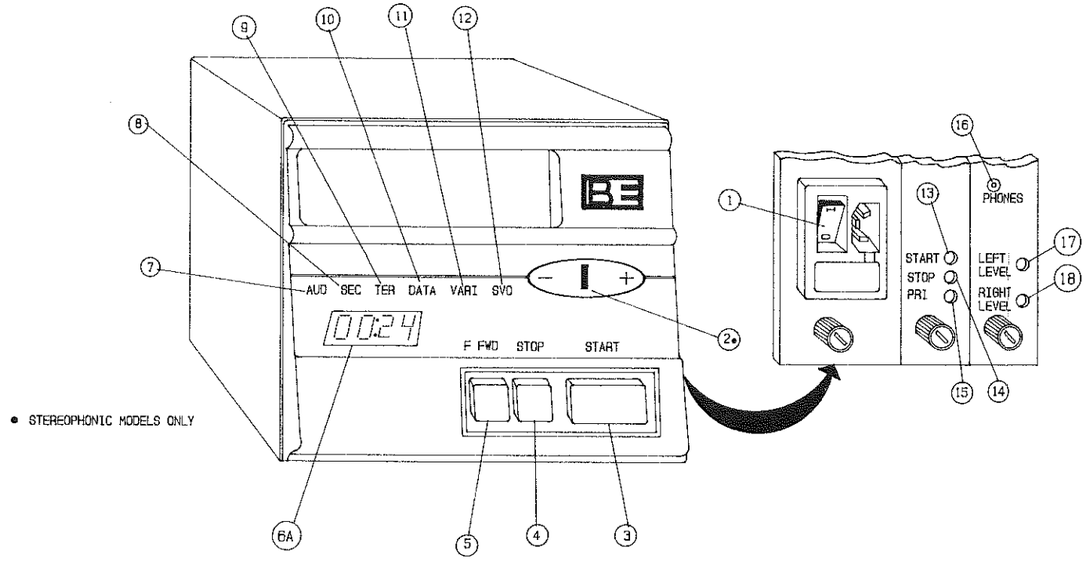
F. On stereophonic models, the phase correction display will begin operation.

TABLE 3–1. CONTROLS AND INDICATORS
(Sheet 1 of 5)

INDEX NO.	NOMENCLATURE	FUNCTION
1	Power Switch	Controls the application of ac power to the unit.
2	Phase Correction Display	A ten–segment multi–color LED display which indicates the relative level of audio phase correction applied to the audio during stereophonic reproduction. Normal operating conditions generate illumination of the green or amber LED segments and intermittent illumination of the red segments. Steady illumination of either red segments are generated by severe audio phase error conditions and indicate the limit of phase correction operations.
3	**START** Switch/ Indicator	SWITCH: A. Initiates tape movement for playback and/ or record operations. B. When momentarily depressed during fast forward operation, returns the unit to the selected operating speed. Audio is enabled when motor is synchronized with the selected operating speed. C. Initiates maintenance mode operation when simultaneously operated with the **STOP** switch/indicator. The motor and solenoid will remain energized for approximately 90 seconds. D. When momentarily depressed in a start lock–out condition, instructs the tape time display to indicate total cartridge tape time. INDICATOR: Illuminates to indicate deck operation.
4	**STOP** Switch/ Indicator	SWITCH: A. Terminates deck operation. B. When momentarily depressed, initiates a motor maintenance mode operation for approximately 90 seconds. C. Initiates maintenance mode operation when simultaneously operated with the **START** switch/indicator. The motor and solenoid will remain energized for approximately 90 seconds. D. Resets start lock–out conditions.



PT-90 RECORD/PLAYBACK UNIT



• STEREOPHONIC MODELS ONLY

PT-90 PLAYBACK UNIT

597-9000-7

FIGURE 3–1.
PT-90 SERIES CONTROLS AND INDICATORS

TABLE 3–1. CONTROLS AND INDICATORS
(Sheet 2 of 5)

INDEX NO.	NOMENCLATURE	FUNCTION
		E. Resets stop indicator flashing conditions. INDICATOR: A. Illuminates to indicate the unit is in the ready mode (unit energized with a cartridge completely inserted into the deck) B. Flashes once per second to indicate a cartridge played condition. C. Flashes twice per second to indicate a cartridge–not–cued condition.
5	**F FWD** Switch/ Indicator	SWITCH: A. When momentarily depressed, initiates fast forward operation. Tape advances at three times the normal speed until a 1 kHz stop tone is detected or the **STOP** switch/ indicator is depressed. Audio is muted. B. When continuously depressed, initiates fast forward operation. Tape advances at three times the normal speed until the switch is released. Audio is enabled. INDICATOR: Illuminates to indicate the unit is in the fast forward mode.
6A	Tape Time Display (Playback Units)	In playback units, displays elapsed message time or total tape time in minutes and seconds. Display operation is terminated when the **STOP** switch/ indicator is depressed or when a primary (1 kHz) stop tone is detected. The tape time display will reset when the cartridge is inserted into the deck. If enabled by circuit programming, the display will also reset when the **START** switch/indicator is depressed. The display will freeze at the beginning or end of an EOM tone depending on circuit programming to display message time and continue operation for total tape time applications.
6B	Tape Time/ Function Display (Record/Playback Units)	In record/playback units, the display is configured for two modes of operation: 1) as a tape time display and 2) as an operating function display. In the tape time mode, the display will operate in an identical manner as described for playback only units (refer to the preceding text). In the operating function mode, the display will indicate the operational parameter of the record/playback unit.

TABLE 3–1. CONTROLS AND INDICATORS
(Sheet 3 of 5)

INDEX NO.	NOMENCLATURE	FUNCTION
7	**AUD** Indicator	Illuminates to indicate audio is enabled.
8	**SEC** Indicator	Illuminates to indicate a secondary (150 Hz) cue tone detection.
9	**TER** Indicator	Illuminates to indicate a tertiary (8 kHz) cue tone detection.
10	**DATA** Indicator	Illuminates to indicate the detection of FSK (3.5 kHz) information.
11	**VARI** Indicator	Illuminates to indicate the unit is operating in the vari–speed mode.
12	**SVO** Indicator	Illuminates to indicate the dc servo motor is not synchronized with the selected operating speed. The **SVO** indicator will momentarily flash when power is initially applied to the motor and during fast forward operation.
13	**START** Indicator	Illuminates to indicate deck operation.
14	**STOP** Indicator	Illuminates to indicate the following: A. Illuminates to indicate the unit is in the ready mode (unit energized with a cartridge completely inserted into the deck). B. Flashes once per second to indicate a cartridge played condition. C. Flashes twice per second to indicate a cartridge–not–cued condition.
15	**PRI** Indicator	Illuminates to indicate the presence of a primary (1 kHz) cue tone.
16	**PHONES** Receptacle	Headphone receptacle.
17	**LEFT LEVEL** Control	Adjusts the left channel audio output level.
18	**RIGHT LEVEL** Control	Adjusts the right channel audio output level.
19	**REC** Switch/Indicator	SWITCH: Configures the unit to the record mode. INDICATOR: A. Illuminates to indicate the unit is in the record mode.

TABLE 3–1. CONTROLS AND INDICATORS
(Sheet 4 of 5)

INDEX NO.	NOMENCLATURE	FUNCTION
		B. Flashes to indicate the unit is in the **LEARN** mode of operation.
20	**TER** Switch	Records an 8 kHz tertiary cue tone on the cue channel for the duration of switch operation. When momentarily depressed, the internal circuitry will generate a 2 ms minimum tertiary cue tone for application to the cue channel. The tertiary cue tone may be recorded when the unit is operating in the playback or record modes.
21	**SEC** Switch	Records a 150 Hz secondary cue tone on the cue channel for the duration of switch operation. When momentarily depressed, the internal circuitry will generate a 100 ms minimum secondary cue tone for application to the cue channel. The secondary cue tone may be recorded when the unit is operating in the playback or record modes.
22	**PRI** Switch/ Indicator	SWITCH: The primary switch/indicator is configured for two modes of operation: 1) initiates primary cue tone record operations and 2) controls the operation of the automatic primary cue tone record circuit. When the switch is depressed during record or play back operation, a 500 ms 1 kHz primary cue tone will be applied to the cue channel. When depressed during the stop mode, the switch controls the operation of the automatic primary cue tone record circuit. INDICATOR: Illuminates to indicate the automatic primary 1 kHz cue tone record circuitry is disabled.
23	**SPL** Switch/ Indicator	SWITCH: Configures the unit to the splice–find mode. The unit will operate to the fast forward mode and automatically stop at the cartridge tape splice. INDICATOR: Illuminates to indicate the unit is configured to the splice–find mode.
24	**ERS** Switch	Configures the unit to erase cue channel audio for the duration of switch operation. Cue channel erase operations may be initiated when the unit is operating in the playback or record mode.

TABLE 3–1. CONTROLS AND INDICATORS
(Sheet 5 of 5)

INDEX NO.	NOMENCLATURE	FUNCTION
25	**MTR** Switch/ Indicator	SWITCH: Configures the front–panel VU meter assembly to display cue audio level information in the left channel meter and bias level information in the right channel meter. INDICATOR: Illuminates to indicate the front–panel VU meter assembly is configured for cue/bias level display operation.
26	**EXEC** Switch	Executes the selected PT–90 record/playback unit operating function.
27	**FCTN** Switch	Selects the desired PT–90 record/playback unit operating function.
28	**DN** Switch	Decrements PT–90 record/playback unit operating parameters such as memory location, fader level, bias level, equalization, and test oscillator frequency.
29	**UP** Switch	Increments PT–90 record/playback unit operating parameters such as memory location, fader level, bias level, equalization, and test oscillator frequency.
30	**VU** Meter Display	A stereophonic multi–color LED display containing VU and peak meter ballistics. Normal display operation provides level indications of record input audio and playback audio. A secondary metering function allows the display to provide indications of cue audio and bias level parameters.
31	**MAN/NORM/LRN** Switch	Selects either manual, normal, or learn modes of PT–90 record/playback unit operation.
32	**LEFT REC** Input Level Control and Indicator	CONTROL: Adjusts the left channel record input level. INDICATOR: Illuminates green to indicate a normal left channel audio input level.
33	**RIGHT REC** Input Level Control and Indicator	CONTROL: Adjusts the right channel record input level. INDICATOR: Illuminates green to indicate a normal right channel audio input level.

3–10. The deck will operate until a primary (1 kHz) stop tone is detected or the deck **STOP** switch/indicator is depressed. When deck operation is terminated, the following events will occur:

A. The **START** switch/indicator will extinguish.

B. The rear–panel **START** indicator will extinguish.

C. The **AUD** indicator will extinguish.

D. The tape time display will indicate the elapsed cartridge tape time.

E. On stereophonic models, the phase correction display will extinguish.

F. The **STOP** switch/indicator will illuminate or flash.

3–11. The PT–90 series cartridge machines are equipped with primary, secondary, and tertiary cue tone detection circuitry. Cue tone detection is indicated as follows:

A. The rear–panel **PRI** indicator will illuminate to indicate the presence of a primary (1 kHz) cue tone.

B. The **SEC** indicator will illuminate to indicate the detection of a secondary (150 Hz) cue tone.

C. The **TER** indicator will illuminate to indicate the detection of a tertiary (8 kHz) cue tone.

3–12. The PT–90 series cartridge machines are also equipped with an FSK decoder circuit. The **DATA** indicator will illuminate to indicate the detection of FSK (3.5 kHz) information.

3–13. **STOP INDICATOR FLASHING.** Stop indicator flashing is designed to provide indications of special operating conditions. If the function is enabled, the **STOP** indicator will flash once per second to indicate a cartridge played condition or twice per second to indicate a cartridge–not–cued condition.

3–14. To reset the **STOP** indicator flashing, depress the **STOP** switch/indicator or remove the cartridge.

3–15. **DECK START LOCK–OUT.** Deck start lock–out is provided to prevent duplicate on–air cartridge play. If the function is enabled, deck start lock–out will be initiated from a cartridge played condition or a cartridge–not–cued condition. Start lock–out operation is indicated to the operator by stop indicator flashing.

3–16. To reset the start lock–out circuitry, remove the cartridge or depress the **STOP** switch/indicator.

3–17. **FAST FORWARD.**

3–18. **MANUAL FAST FORWARD.** The manual fast forward feature may be operated with the muting circuit enabled or disabled. To operate the unit in the manual fast forward mode with audio muted, momentarily depress the front–panel **F FWD** switch/indicator. To operate the unit in the manual fast forward mode with audio enabled, continuously depress the **F FWD** switch/indicator. The **F FWD** switch/indicator will illuminate to indicate the fast forward circuitry is enabled. Fast forward advance will continue until a stop tone is detected, the **STOP** switch/indicator is depressed, or the **START** switch/indicator is depressed. Once fast forward operation is terminated, the **STOP** switch/indicator will illuminate or flash.

3–19. **AUTOMATIC FAST FORWARD.** To operate the unit in the automatic fast forward mode, the appropriate circuitry on the logic circuit board must be enabled. Insert the cartridge into the deck and initiate playback operation. When an EOM is detected, the unit will operate to fast forward advance with audio muted. Fast forward advance will continue until a stop tone is detected, the **STOP** switch/indicator is depressed, or the **START** switch/indicator is depressed. Once fast forward operation is terminated, the **STOP** switch/indicator will illuminate or flash.

3–20. TAPE TIME DISPLAY OPERATION.

3–21. The PT–90 playback tape time display and the PT–90 record/playback tape time/function display normally indicate elapsed message time. The display will also indicate total cartridge tape time if desired. At a EOM detection, the tape time display will freeze to indicate message time and continue operation for total tape time applications. The unit will indicate total tape time only when in a start lock–out condition. To display total tape time, momentarily depress the **START** switch/indicator when the unit is in a start lock–out condition.

3–22. ELEVATED LEVEL CARTRIDGE SENSING OPERATION.

3–23. The PT–90 series cartridge machines are equipped with an elevated level cartridge sensor. If elevated level cartridge detection is required, attach a reflective label (supplied in the accessory parts kit) to the cartridge near the capstan shaft opening for tapes recorded at a 250 nWb/m level.

3–24. MAINTENANCE MODE OPERATION.

3–25. All PT–90 cartridge machines are equipped with a maintenance mode feature which energizes the motor or motor and solenoid to allow routine pressure roller and capstan shaft cleaning. To generate a motor only maintenance mode command, remove any tape cartridge and momentarily depress the **STOP** switch/indicator. The motor will energize for approximately 90 seconds and terminate operation automatically. To generate a motor and solenoid maintenance mode command, remove any tape cartridge and simultaneously depress the **START** and **STOP** switch/indicators and release the **STOP** switch/indicator prior to the **START** switch/indicator. The motor and solenoid will energize for approximately 90 seconds and terminate operation automatically.

3–26. AUDIO MONITORING.

3–27. A miniature headphone receptacle is provided for monitoring the cartridge machine audio output. To monitor the audio output, insert high impedance headphones into the **PHONES** receptacle.

3–28. RECORD OPERATION.

3–29. **GENERAL.** PT–90 record/playback units are equipped with three modes of operation: 1) normal, 2) learn, and 3) manual. The modes provide an increasing level of operating functions. This allows the operator to select the desired level for the type of operation to be performed.

3–30. The first level of operation is the normal mode. The normal mode provides tape time display and recall memory functions. Each record/playback unit is equipped with the ability to establish and store record compensation data for a specific type of tape to be used. The recall memory function allows the operator to access the stored information for accurate and convenient record operations. The tape time display function indicates elapsed message time and total tape time information.

3–31. The second level of operation is the learn mode. The learn mode provides the operating characteristics of the normal mode with the additional function of automatic record alignment. In the learn mode, the unit operates in a self–alignment mode to evaluate and establish record bias, record equalization, and record level parameters for optimum performance from a specific type of tape. The record compensation data is stored in memory for convenient operator recall when required. Up to 10 sets of record compensation characteristics may be stored in memory.

3–32. The third level of operation is the manual mode. The manual mode provides the operating characteristics of the normal and learn modes with the addition of manual record compensation functions. Manual record compensation functions include: 1) fader level control, 2) bias level control, 3) high frequency equalization control, 4) save memory operation, 5) test oscillator operation, and 6) A–to–D converter alignment. The manual mode allows the operator to manually align the unit for specific record compensation characteristics and for maintenance procedures.

3–33. **NORMAL MODE.** The normal mode of operation is designed for general record operations. Figure 3–2 presents the normal mode controls and operating functions. The normal mode provides tape time display and recall memory operations. To select operating functions in the normal mode, proceed as follows.

3–34. Operate the rear–panel power switch to on.

3–35. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to NORM and insert a cartridge into the deck.

3–36. **Tape Time Display Operation.** To operate the unit for tape time display operations, proceed as follows:

3–37. Operate the **FCTN** switch until the tape time/function display indicates T000. The display will indicate elapsed message time or total cartridge tape time information. Refer to the TAPE TIME DISPLAY OPERATION in the preceding text for tape time display operating functions.

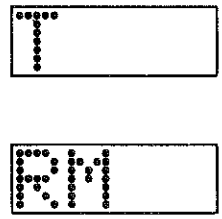
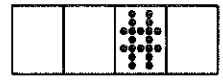
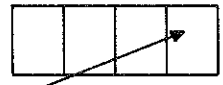
3–38. **Recall Memory Operation.** To operate the unit to access stored record compensation characteristics, proceed as follows:

3–39. Operate the **FCTN** switch until the tape time/function display indicates RM____ .

3–40. Select a set of record compensation characteristics stored in memory locations 1 through 9 or E by operating the **UP** or **DN** switches as required until the forth digit of the tape time/function display indicates the desired memory location.

EXAMPLE:

3–41. Depress the **EXEC** switch to execute the recall memory operation. A # symbol in the third digit of the tape time/function display will illuminate to indicate execution of the recall memory operation.

NORMAL MODE OPERATION				
INDEX NO.	SWITCH NOMENCLATURE	DESCRIPTION	FUNCTION	DISPLAY NOMENCLATURE
1	FCTN SWITCH	CONFIGURES THE UNIT FOR TAPE TIME DISPLAY OR RECALL MEMORY OPERATION.	TAPE TIME DISPLAY- DISPLAYS TAPE TIME INFORMATION RECALL MEMORY- ACCESSES MEMORY LOCATIONS 1 THROUGH 9 OR E TO RECALL RECORD COMPENSATION CHARACTISTICS.	
2	EXEC SWITCH	INSTRUCTS THE UNIT TO EXECUTE THE SELECTED FUNCTION.		
3	UP AND DN SWITCHS	SELECTS MEMORY LOCATIONS 1 THROUGH 9 OR E IN THE RECALL MEMORY MODE.		 SINGLE-DIGIT MEMORY LOCATION DISPLAY. MEMORY LOCATION PARAMETERS: 1 THROUGH 9 OR E.

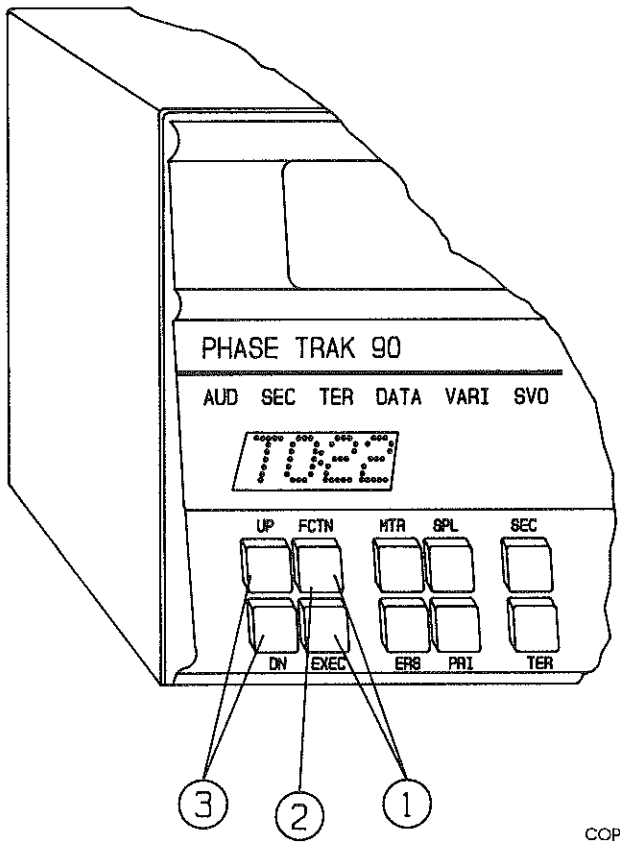


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FIGURE 3-2. NORMAL MODE CONTROLS AND FUNCTIONS

3–42. **LEARN MODE.** The learn mode provides the ability to automatically generate sets of record compensation characteristics. The operating mode is designed for evaluation and storage of record compensation characteristics of each type of tape in a station tape cartridge system. Figure 3–3 presents learn mode controls and operating functions. The learn mode provides the operating characteristics of the normal mode with the addition of automatic record compensation generation. To operate the unit in the learn mode, proceed as follows.

3–43. Operate the rear–panel power switch to on.

3–44. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to LRN.

3–45. Select a tape cartridge for learn mode operation which contains: 1) a minimum of 1 minute of tape and 2) the type of tape required for evaluation. Erase the selected tape cartridge completely. The cartridge must be completely erased for proper learn mode operation. Insert the bulk erased tape cartridge into the deck.

3–46. Depress and hold the **EXEC** switch, then depress the **FCTN** switch. The tape time/function display will indicate LRN__ . The **RECORD** switch/indicator will flash.

3–47. Select memory location 1 through 9 or E for placement of the record compensation data by operating the **UP** or **DN** switches as required until the fourth digit of the tape time/function display indicates the desired memory location.

EXAMPLE:

3–48. Initiate learn mode operation by depressing the **START** switch/indicator to illuminate the switch/indicator. The **RECORD** switch/indicator will illuminate. The unit will evaluate the tape and generate a set of record compensation characteristics. When learn operation is complete, the unit will: 1) terminate operation automatically, 2) illuminate the **STOP** switch/indicator, 3) store the record characteristics in the selected memory location, and 4) extinguish the **REC** switch/indicator.

3–49. If during learn mode operation the tape cartridge requires compensation which exceeds preset operating parameters, the unit will terminate operation and the tape time/function display will indicate FAIL. If this condition occurs, remove the defective tape cartridge from the deck. Select a different cartridge for evaluation and repeat the learn mode procedure.

LEARN MODE OPERATION				
INDEX NO.	SWITCH NOMENCLATURE	DESCRIPTION	FUNCTION	DISPLAY
1	FCTN AND EXEC SWITCHES	CONFIGURES THE UNIT FOR LEARN MODE OPERATION.	LEARN- AUTOMATICALLY GENERATES RECORD COMPENSATION CHARACTERISTICS. IF DURING LEARN MODE OPERATION THE TAPE REQUIRES COMPENSATION WHICH EXCEEDS PRESET OPERATING PARAMETERS, THE DISPLAY WILL INDICATE FAIL.	LEARN FAIL
2	UP AND DN SWITCHES	SELECTS MEMORY LOCATION 1 THROUGH 9 OR E FOR STORAGE OF RECORD COMPENSATION CHARACTERISTICS.		SINGLE-DIGIT MEMORY LOCATION DISPLAY. MEMORY LOCATION PARAMETERS: 1 THROUGH 9 OR E.
ADDITIONAL LEARN MODE FUNCTIONS- NORMAL MODE OPERATIONS MAY BE INITIATED FROM THE LEARN MODE. REFER TO NORMAL MODE OPERATING PROCEDURES.				

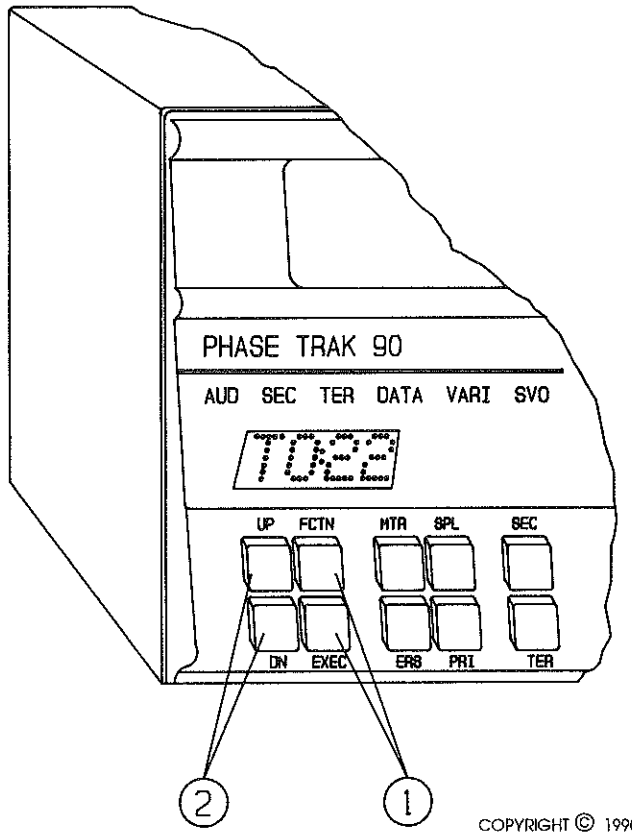

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FIGURE 3-3. LEARN MODE CONTROLS AND FUNCTIONS

3–50. If manual termination of the learn mode is required, operate the **STOP** switch/indicator to illuminate the switch/indicator. The tape time/function display will indicate T___.

3–51. **Additional Learn Mode Operations.** Tape time display and recall memory operations associated with normal mode operation may be initiated from the learn mode. If tape time display or recall memory operations are required, refer to the NORMAL MODE operating procedures in the preceding text.

3–52. **MANUAL MODE.** Manual mode operation allows the operator to manually align the unit for specific record compensation characteristics and maintenance procedures. Figure 3–4 presents manual mode controls and operating functions. The manual mode provides the operating characteristics of the normal and learn modes of operation with the addition of manual record compensation functions.

3–53. The following text provides operating procedures for bias level, fader level, equalization, save memory, test oscillator, and A–to–D converter alignment operating functions. The bias level, fader level, and the equalization procedures must be performed and the save memory function executed to store the characteristics in memory. To operate the unit in the manual mode, proceed as follows:

3–54. Operate the rear–panel power switch to On.

3–55. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to MAN.

3–56. Select a bulk erased tape cartridge which contains: 1) a minimum of 1 minute of tape and 2) the type of tape required for evaluation. Insert the bulk erased tape cartridge into the deck.

3–57. Manual mode operations such as bias and fader level alignments may be performed using the front–panel VU meter. If increased resolution is desired, connect an external VU to the unit left channel output receptacle.

3–58. **Test Oscillator.** The test oscillator mode is provided for manual record compensation operations and maintenance procedures. To operate the test oscillator, proceed as follows:

3–59. Operate the **FCTN** switch until the tape time/function display indicates OFF.

3–60. The **UP** and **DN** switches select the test oscillator frequencies. The following list presents the available test oscillator frequencies. Operate the **UP** and **DN** switches as required to select a test oscillator frequency. The tape time/function display will indicate the selected test frequency (refer to example below).

TEST FREQUENCIES

1.	50	5.	4K
2.	125	6.	8K
3.	500	7.	12K
4.	1K	8.	16K

EXAMPLE:

3–61. Operate the **RECORD** switch/indicator to illuminate the switch/indicator.

3–62. Operate the **START** switch/indicator to illuminate the switch/indicator.

3–63. The test oscillator may be configured for sweep–up and sweep–down operations. To configure the oscillator for sweep–up operation, depress and hold the **UP** switch for approximately 3 seconds. The tape time/function display will indicate the frequencies during sweep–up operation. To configure the oscillator for sweep–down operation, depress and hold the **DN** switch for approximately 3 seconds. The tape time/function display will indicate frequencies during sweep–down operation.

3–64. **Record Bias.** To manually adjust the record bias, proceed as follows:

3–65. Refer to the **Test Oscillator** operating procedure in the preceding text and select a record bias test frequency. For optimum performance, it is recommended the record bias alignment be performed at 12 kHz.

3–66. Configure the unit for record bias operations by operating the **FCTN** switch until the tape time/function display indicates B___. Tape time/function display digits 2 through 4 will indicate random record bias parameters.

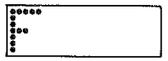
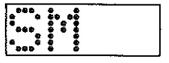
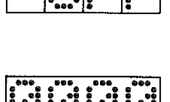
3–67. The **EXEC** switch configures the unit for left channel or right channel operating parameters. Operate the **EXEC** switch until the second digit of the tape time/function display indicates L. With the assignment of left channel operating parameter, the tape time/function display will indicate BL__.

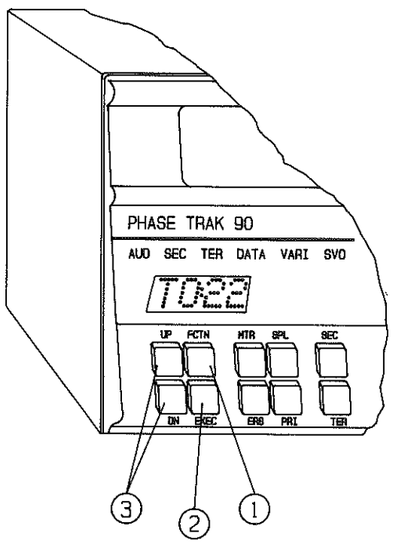
3–68. Operate the **RECORD** switch/indicator to illuminate the switch/indicator.

3–69. Operate the **START** switch/indicator to illuminate the switch/indicator.

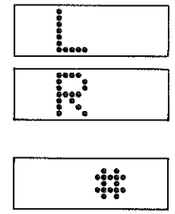
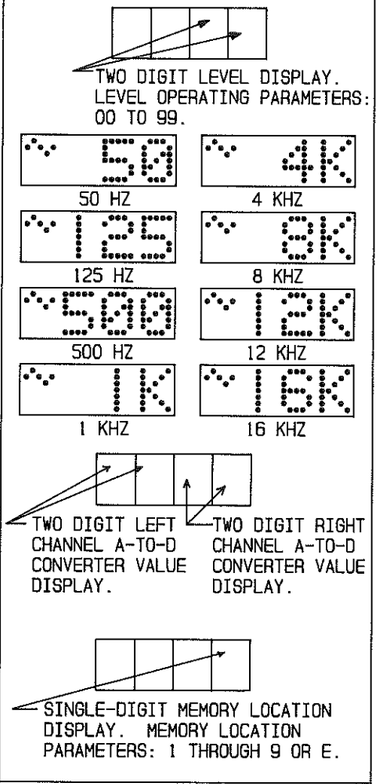
3–70. The **UP** and **DN** switches adjust the record bias level. The third and forth digits of the tape time/function display will indicate a record bias value from 0 to 99 (refer to the example below). Operate the **UP** and **DN** switches as required to establish the left channel record bias as desired. For optimum performance, it is recommended the record bias be adjusted to obtain a peak indication on the front–panel VU meter. Once the peak indication is obtained, increase the bias level by depressing the **UP** switch until the front–panel VU meter decreases 2 dB.

MANUAL MODE OPERATION

INDEX NO.	SWITCH NOMENCLATURE	DESCRIPTION	FUNCTION	DISPLAY
1	FCTN SWITCH	SELECTS THE FOLLOWING MANUAL MODE OPERATING FUNCTIONS: 1. NORMAL MODE OPERATIONS: (TAPE TIME DISPLAY AND RECALL MEMORY) 2. FADER LEVEL 3. BIAS LEVEL 4. EQUALIZATION LEVEL 5. SAVE MEMORY 6. TEST OSCILLATOR 7. A-TO-D CONVERTER ALIGNMENT	FADER LEVEL- CONTROLS THE FADER LEVEL. THE FADER LEVEL IS REPRESENTED BY A NUMERICAL VALUE FROM 00 TO 99. BIAS LEVEL- CONTROLS THE RECORD BIAS LEVEL. THE BIAS LEVEL IS REPRESENTED BY A NUMERICAL VALUE FROM 00 TO 99. EQUALIZATION- CONTROLS THE HIGH FREQUENCY EQUALIZATION. THE EQUALIZATION LEVEL IS REPRESENTED BY A NUMERICAL VALUE FROM 00 TO 99. SAVE MEMORY- CONFIGURES THE UNIT TO STORE RECORD COMPENSATION CHARACTERISTICS IN MEMORY. TEST OSCILLATOR- CONTROLS THE OPERATION OF THE INTERNAL TEST OSCILLATOR. A-TO-D CONVERTER ALIGNMENT- A MAINTENANCE PROCEDURE WHICH ALIGNS THE INTERNAL A-TO-D CONVERTER.	    



MANUAL MODE OPERATION

INDEX NO.	SWITCH NOMENCLATURE	DESCRIPTION	FUNCTION	DISPLAY
2	EXEC SWITCH	1. SELECTS EITHER THE LEFT CHANNEL OR RIGHT CHANNEL OPERATING PARAMETER FOR MANUAL MODE FUNCTIONS. 2. INSTRUCTS THE UNIT TO EXECUTE A SAVE MEMORY OPERATION.		
3	UP AND DN SWITCHES	1. SELECTS LEVEL PARAMETERS FOR FADER, BIAS AND EQUALIZATION MODES OF OPERATION. 2. SELECTS TEST OSCILLATOR FREQUENCIES FOR TEST OSCILLATOR OPERATION. 3. SELECTS LEVEL PARAMETERS FOR A-TO-D CONVERTER ALIGNMENT OPERATION. 4. SELECTS MEMORY LOCATIONS 1 THROUGH 9 OR E FOR SAVE MEMORY OPERATIONS.		 TWO DIGIT LEVEL DISPLAY. LEVEL OPERATING PARAMETERS: 00 TO 99. 50 HZ, 4 KHZ, 125 HZ, 8 KHZ, 500 HZ, 12 KHZ, 1 KHZ, 16 KHZ TWO DIGIT LEFT CHANNEL A-TO-D CONVERTER VALUE DISPLAY. TWO DIGIT RIGHT CHANNEL A-TO-D CONVERTER VALUE DISPLAY. SINGLE-DIGIT MEMORY LOCATION DISPLAY. MEMORY LOCATION PARAMETERS: 1 THROUGH 9 OR E.

ADDITIONAL MANUAL MODE FUNCTIONS-
NORMAL AND LEARN MODES OF OPERATION MAY BE INITIATED FROM THE MANUAL MODE. REFER TO NORMAL AND LEARN MODE OPERATION PROCEDURES.

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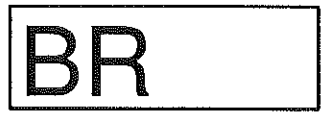
FIGURE 3–4.
MANUAL MODE CONTROLS AND INDICATORS

EXAMPLE:

3–71. Repeat the procedure for the right channel. The unit is configured for right channel operation by depressing the **EXEC** switch until the second digit of the tape time/function display indicates R. With the assignment of right channel operating parameter, the tape time/function display will indicate BR__.



3–72. **Fader Level.** To manually adjust the record input level, proceed as follows:

3–73. Refer to the **Test Oscillator** operating procedure in the preceding text and select a record input level test frequency. For optimum performance, it is recommended the record input level alignment be performed at 1 kHz.

3–74. Configure the unit for input level adjustment by operating the **FCTN** switch until the tape time/function display indicates F___. Tape time/function display digits 2 through 4 will indicate random fader level parameters.

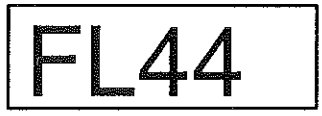
3–75. The **EXEC** switch configures the unit for left channel or right channel parameters. Operate the **EXEC** switch until the second digit of the tape time/function display indicates L. With the assignment of left channel operating parameter, the tape time/function display will indicate FL__.

3–76. Operate the **RECORD** switch/indicator to illuminate the switch/indicator.

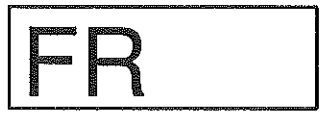
3–77. Operate the **START** switch/indicator to illuminate the switch/indicator.

3–78. The **UP** and **DN** switches adjust the record fader level. The third and forth digits of the tape time/function display will indicate a fader value from 0 to 99 (refer to the example below). Operate the **UP** and **DN** switches as required to establish the left channel record input level as desired. For optimum performance, it is recommended the record input level be adjusted to obtain a front–panel VU meter indication of 0 dB.

EXAMPLE:



3–79. Repeat the procedure for the right channel. The unit is configured for right channel operation by depressing the **EXEC** switch until the second digit of the tape time/function display indicates R. With the assignment of right channel operating parameter, the tape time/function display will indicate FR__.



3–80. **Equalization.** To manually adjust the high frequency equalization, proceed as follows:

3–81. Refer to the **Test Oscillator** operating procedure in the preceding text and select a high frequency equalization test frequency. For optimum performance, it is recommended equalization be performed at 12 kHz.

3–82. Configure the unit for equalization by operating the **FCTN** switch until the tape time/function display indicates E___. Tape time/function display digits 2 through 4 will indicate random equalization parameters.

3–83. The **EXEC** switch configures the unit for left channel or right channel operating parameters. Operate the **EXEC** switch until the second digit of the tape time/function display indicates L. With the assignment of the left channel operating parameter, the tape time/function display will indicate EL__.

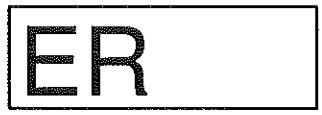
3–84. Operate the **RECORD** switch/indicator to illuminate the switch/indicator.

3–85. Operate the **START** switch/indicator to illuminate the switch/indicator.

3–86. The **UP** and **DN** switches adjust the high frequency equalization. The third and forth digits of the tape time/function display will indicate an equalization value from 0 to 99 (refer to the example below). Operate the **UP** and **DN** switches as required to obtain the level established in the **Fader Level** adjustment procedure.

EXAMPLE:

3–87. Repeat the procedure for the right channel. The unit is configured for right channel operation by depressing the **EXEC** switch until the tape time/function display indicates ER__. With the assignment of the right channel operating parameter, the tape time function will indicate ER__.



3–88. **Save Memory.** The save memory function stores the record bias level, fader level, and equalization level parameters in memory. To store the record compensation parameters in memory, proceed as follows:

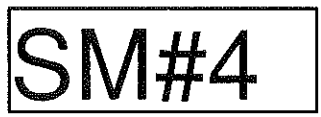
3–89. Configure the unit to the save memory mode by operating the **FCTN** switch until the tape time/function display indicates SM__. Tape time/function display digits 3 and 4 will indicate random save memory parameters.

3–90. Select memory location 1 through 9 or E by operating the **UP** or **DN** switches as required until the forth digit of the tape time/function display indicates the desired memory location.

EXAMPLE:

3–91. Depress the **EXEC** switch to store the record compensation characteristics in the selected memory location. A # symbol in the third digit of the tape time/function display will illuminate to indicate the execution of the save memory function.

EXAMPLE:



3–92. **A–To–D Converter Alignment.** An A–to–D converter alignment function is provided for A–to–D converter maintenance. The tape time/function display will illuminate 0000 to indicate A–to–D converter mode operation. If A–to–D converter alignment is required, refer to SECTION V, MAINTENANCE and perform the A–TO–D CONVERTER ALIGNMENT procedure.

3–93. **Additional Manual Mode Operations.** Tape time display and recall memory operations associated with the normal mode and all learn mode operations may be initiated from the manual mode. If tape time display, recall memory, or learn mode operations are required, refer to the NORMAL MODE and LEARN MODE operating procedures in the preceding text.

3–94. **SPLICE–FIND MODE.** The splice–find mode allows the operator to conveniently find cartridge tape splices for record operations. Splice–find operation may be initiated from the manual, normal, or learn modes of operation. To operate the unit for splice–find operation, proceed as follows:

3–95. Select a tape cartridge for splice–find operation and insert the cartridge into the deck.

3–96. Operate the **SPL** switch/indicator to illuminate the switch/indicator. The unit will operate to fast forward advance and automatically stop just beyond the cartridge tape splice. The **STOP** switch/indicator will illuminate.

3–97. **ERASE OPERATION.** The PT–90 record/playback unit is equipped with an erase mode for cue channel erase operations. Cue channel erase operations may be initiated from the normal, learn, or manual modes during playback operation. To operate the unit for cue channel erase operations, proceed as follows:

3–98. Select a tape cartridge for cue channel erase operation and insert the cartridge into the deck.

3–99. Operate the **START** switch/indicator to illuminate the switch/indicator and begin tape movement.

3–100. Depress and hold the **ERS** switch to erase the cue channel information as required.

3–101. Operate the **STOP** switch/indicator to illuminate the switch/indicator.

3–102. **VU METER OPERATION.** The multi–color LED VU meter display normally indicates playback audio level information during playback operation and record input/playback audio level information during record operations. The level display will also indicate cue channel level and bias level information if required.

3–103. To configure the meter to display cue channel level and bias level information, operate the **MTR** switch/indicator to illuminate the switch/indicator. The VU meter left channel display will indicate cue channel level playback information during playback operation or cue audio input information during record operation. The VU meter right channel display will indicate specific cue bias level parameters for the following conditions:

A. In the record mode, the level meter right channel display will indicate the sum of the left channel, right channel, and cue bias levels.

B. In the playback mode, the level meter right channel display will indicate cue bias level information.

C. When the **ERS** switch is depressed, the level meter right channel display will indicate the erase bias.

3–104. **RESET OPERATION.** The PT–90 record/play unit is equipped with a microprocessor reset function. To reset the cartridge machine, simultaneously depress the **REC** and **EXEC** switches.

3–105. **RECORDING PROGRAM MATERIAL.** To operate the PT–90 record/playback unit for program record operations, proceed as follows:

3–106. Select the program material to be recorded. Ensure the playback system output level is within the PT–90 record/playback unit input level specifications.

3–107. Select a bulk erased cartridge that is approximately 2 seconds longer than the selected material to be recorded.

3–108. Operate the rear–panel power switch to on.

3–109. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to NORM.

3–110. Refer to the SPLICE–FIND operating procedures in the preceding text and operate the unit to find the cartridge tape splice.

3–111. Select the type of primary cue tone record operation. For automatic primary cue tone record operations, operate the **PRI** switch/indicator to extinguish the switch/indicator. For manual primary cue tone record operations, operate the **PRI** switch/indicator to illuminate the switch/indicator.

3–112. Select a desired set of record compensation characteristics as follows:

A. Operate the **FCTN** switch until the tape time/function display indicates RM__.

B. Operate the **UP** or **DN** switches as required until the fourth digit of the tape time/function display indicates the memory location of the desired set of record compensation characteristics.

EXAMPLE:

3–113. Depress the **EXEC** switch to execute the recall memory operation. A # symbol in the third digit of the tape time/function display will illuminate to indicate execution of the function.

3–114. Coarse adjust the record input level by starting the program material and adjusting the **LEFT REC LEVEL** and **RIGHT REC LEVEL** controls to illuminate the input level indicators.

3–115. Operate the **REC** switch/indicator to illuminate the switch/indicator.

3–116. Operate the **START** switch/indicator to illuminate the switch/indicator and start the playback system to begin recording program material. If the automatic primary cue tone record function is enabled, a stop tone will be automatically recorded on the cue channel. The front–panel VU meter will indicate record input audio or playback audio depending on circuit programming.

3–117. At the end of the record operations, depress the **PRI** switch/indicator to record a primary cue tone if the automatic primary cue tone record function is disabled. Record operation will terminate automatically when a primary cue tone is detected. To terminate record operation manually, depress the **STOP** switch/indicator. The **STOP** switch/indicator will illuminate or flash. The **REC** switch/indicator will extinguish.

3–118. **SECONDARY AND TERTIARY CUE TONE RECORDING.** Secondary and tertiary cue tone recording may be initiated during playback or record operation. To record secondary or tertiary cue tones, proceed as follows:

3–119. Operate the record/playback unit in the record or playback mode.

3–120. Depress the **SEC** switch or **TER** switch for the amount of time the tone is desired. Do not record a secondary or tertiary cue tone of less than one second.

3–121. **FSK ENCODING.** To operate the PT–90 record/playback unit for FSK encoding, proceed as follows.

3–122. **Manual FSK Encoding.** For manual FSK encoding systems. proceed as follows:

3–123. FSK text composition is performed on the encoding system computer/data terminal. For systems configured with a personal computer, the text editing software must be configured to print data to the computer serial port. Refer to the applicable software package operation manual and configure the computer for serial port printing.

3–124. Operate the encoding system computer/data terminal to compose the FSK text. Once the text is created, perform the computer/data terminal printing procedures with the exception of the final print command.

3–125. Apply power to the cartridge machine and insert the tape cartridge for FSK encoding into the deck.

3–126. Depress the cartridge machine start switch/indicator to initiate deck operation. Wait approximately one second to allow the cartridge machine operation to stabilize and operate the computer/data terminal for a final print command. The FSK data will be routed through the computer/data terminal to the cartridge machine for application to the cartridge cue track. The cartridge machine will terminate operation when a primary cue tone is detected.

3–127. **Automatic FSK Encoding.** For automatic FSK encoding systems, proceed as follows:

3–128. Insert the disk containing the FSK data encoder software program into the disk drive and load the program. When the loading process is complete, refer to the HELP screen for operating instructions.

3–129. Ensure the interface cable is connected between the PT–90 and personal computer as shown in Figure 2–8 in SECTION II, INSTALLATION. Apply power to the cartridge machine and insert the tape cartridge for FSK encoding into the deck.

3–130. Select the desired text editor and compose the FSK information. To begin the encoding process, operate the appropriate keyboard command (refer to the HELP screen). The PT–90 will record the FSK data on the cartridge cue track and terminate operation when a primary cue tone is detected.

3–131. To obtain a printed copy of the installation information, enter the following command and depress the return key.

PT90.DOC> PRN

SECTION IV
THEORY OF OPERATION

4–1. INTRODUCTION.

4–2. This section presents the theory of operation for the Broadcast Electronics PT–90 series cartridge machines. Figure 4–1 presents a detailed block diagram of the PT–90 playback circuitry. Figure 4–2 presents a detailed block diagram of the PT–90 record circuitry. Refer to Figures 4–1 and 4–2 as required for the following equipment description.

4–3. GENERAL DESCRIPTION.

4–4. All PT–90 cartridge machines are equipped with a direct drive dc servo motor, a precision–manufactured deck assembly, and solid–state electronics. The dc servo motor system and the deck assembly provide precise tape movement for accurate audio reproduction. The playback unit electronics are implemented on six circuit board assemblies: 1) power supply, 2) motor control, 3) front panel, 4) logic, 5) motherboard, and 6) audio. The record/playback unit electronics include the playback power supply, motor control, logic, and audio assemblies with the addition of the following record assemblies: 1) motherboard, 2) front panel, 3) record preamplifier, 4) record bias, and 5) CPU. The logic, audio, power supply, record preamplifier, record bias, and CPU assemblies are plug–in modules designed for ease of service.

4–5. PLAYBACK CIRCUITRY.

4–6. **TAPE TRANSPORT SYSTEM.** The PT–90 tape transport system consists of a direct drive dc servo motor and a precision–manufactured deck assembly. The brushless dc motor is mounted directly to the cartridge deck with the capstan shaft extending vertically upward through the deck for direct drive operation. Precision control of motor operations is provided by the motor control circuit board. The dc servo motor system exhibits precise motor operation for accurate tape movement.

4–7. The cartridge machine deck assembly is equipped with a cartridge guidance system, an air–damped solenoid, a deck microswitch, an elevated level tape sensor, and the Broadcast Electronics PHASE LOCK V head assembly. The cartridge guidance system consists of several spring–loaded components designed to channel a cartridge into the proper play position. The air–damped solenoid is designed for high tape pulling force and provides a rapid response to start commands. A deck microswitch generates a ready status signal for application to the start logic when a cartridge is inserted into the deck. An infrared sensor is incorporated into the deck design to indicate the presence of an elevated level cartridge.

4–8. The Broadcast Electronics PHASE LOK V head assembly is a modular device designed to provide the tape heads with a mechanically secure and stable environment. The head assembly permits independent adjustment of the head height/zenith and head azimuth. Locking components for the head adjustment controls and the unique head assembly design act to maintain tape head alignment. Due to the modular design, the entire PHASE LOK V assembly may be removed from the deck for alignment or service.

4–9. **POWER SUPPLY MODULE.** The PT–90 power supply module is a self–contained power supply device designed for ease of maintenance. The module is equipped with: 1) an ac input receptacle, 2) a toroid power transformer, 3) rectifier and filter circuitry, and 4) a solenoid driver circuit. The power supply module is designed to accept either 110V or 220V ac input potentials.

4–10. Primary ac power is applied to the PT–90 cartridge machine through the ac input receptacle. The ac input receptacle is equipped with built–in ac power control and overload protection components. Primary ac power conversion is accomplished by a toroid power transformer. DC power conversion is accomplished by positive and negative rectifier and filter networks. A programmable grounding network isolates and distributes ground circuits for special applications. A solenoid driver circuit functions to initiate and maintain solenoid operation.

4–11. **DC SERVO MOTOR.** The cartridge machine motor is a dc servo type constructed in a three stator wye configuration. Each stator is equipped with a hall effect sensor and a permanent magnet. The hall effect sensors are strategically placed in the motor assembly to accurately monitor and control stator operation. The motor is also equipped with a tachometer winding which routes motor speed information to the motor control circuit.

4–12. The sensors operate on the hall effect principle which refers to a voltage developed between two metallic strips when passed through a magnetic field. Each sensor outputs a varying dc voltage which is proportional to the magnetic field in the winding. The voltage is routed to the motor control circuit board as feedback for stator control.

4–13. **MOTOR CONTROL CIRCUIT BOARD.** The motor control circuit board and the cartridge machine motor function as a closed–loop dc servo motor system. The motor control circuit acts to initiate and maintain motor operation to a high degree of precision. The control circuitry also protects the motor from over–current and loss–of–reference conditions.

4–14. A precision reference signal for servo control operations is generated by a crystal oscillator circuit. The reference signal and motor speed information are routed to a frequency comparator. The comparator evaluates the information and outputs a corresponding control signal to the motor driver circuit. The driver circuit processes the signal and outputs dc control information to the motor. A commutator circuit functions to control motor operation by processing and routing the hall effect sensor information to the motor windings. Motor braking operations are controlled by a motor brake control circuit and the motor commutator circuit.

4–15. **FRONT PANEL DISPLAY CIRCUIT BOARD.** The playback unit phase correction display and tape time display are housed on the front panel display circuit board. The front panel display circuit board also contains the **AUD, SEC, TER, DATA, VARI,** and **SVO** indicators.

4–16. **MOTHERBOARD ASSEMBLY.** The PT–90 motherboard assembly provides all required internal circuit communication. The motherboard assembly also distributes audio, elevated level cartridge sensor, and deck status information to the proper circuit board assemblies.

4–17. **AUDIO MODULE.** The PT–90 playback audio circuitry is housed on the audio module. Stereophonic units are equipped with left and right channel audio circuits and automatic phase correction circuitry. Monophonic units are equipped with only the left channel audio circuit.

4–18. Each audio channel is equipped with an amplifier/equalization stage. The amplifier/equalization stage is designed to provide ±6 dB low frequency equalization, ±10 dB high frequency equalization, and an overall a gain of approximately 50 dB.

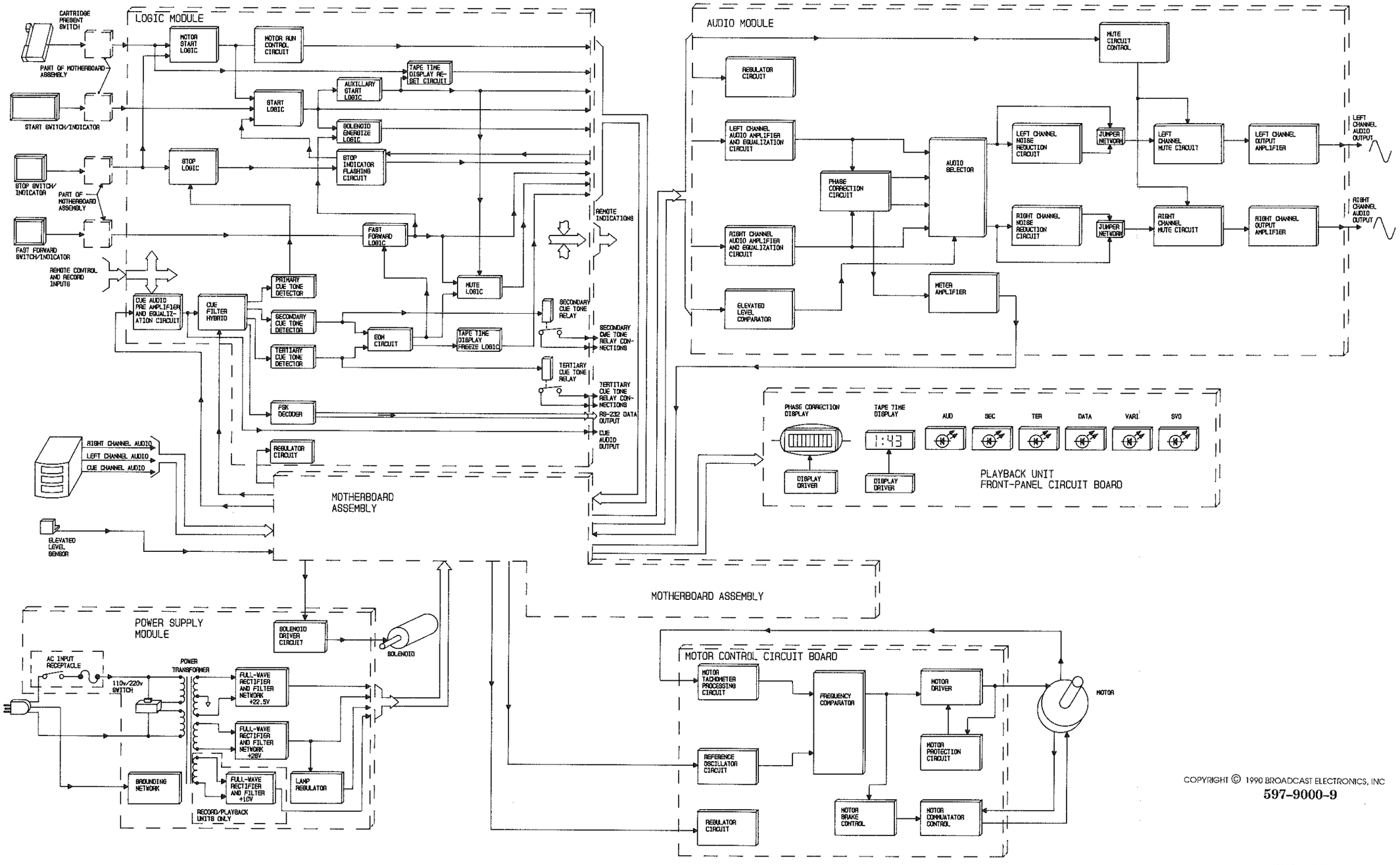


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FIGURE 4–1.
PT–90 BLOCK DIAGRAM, PLAYBACK CIRCUITRY

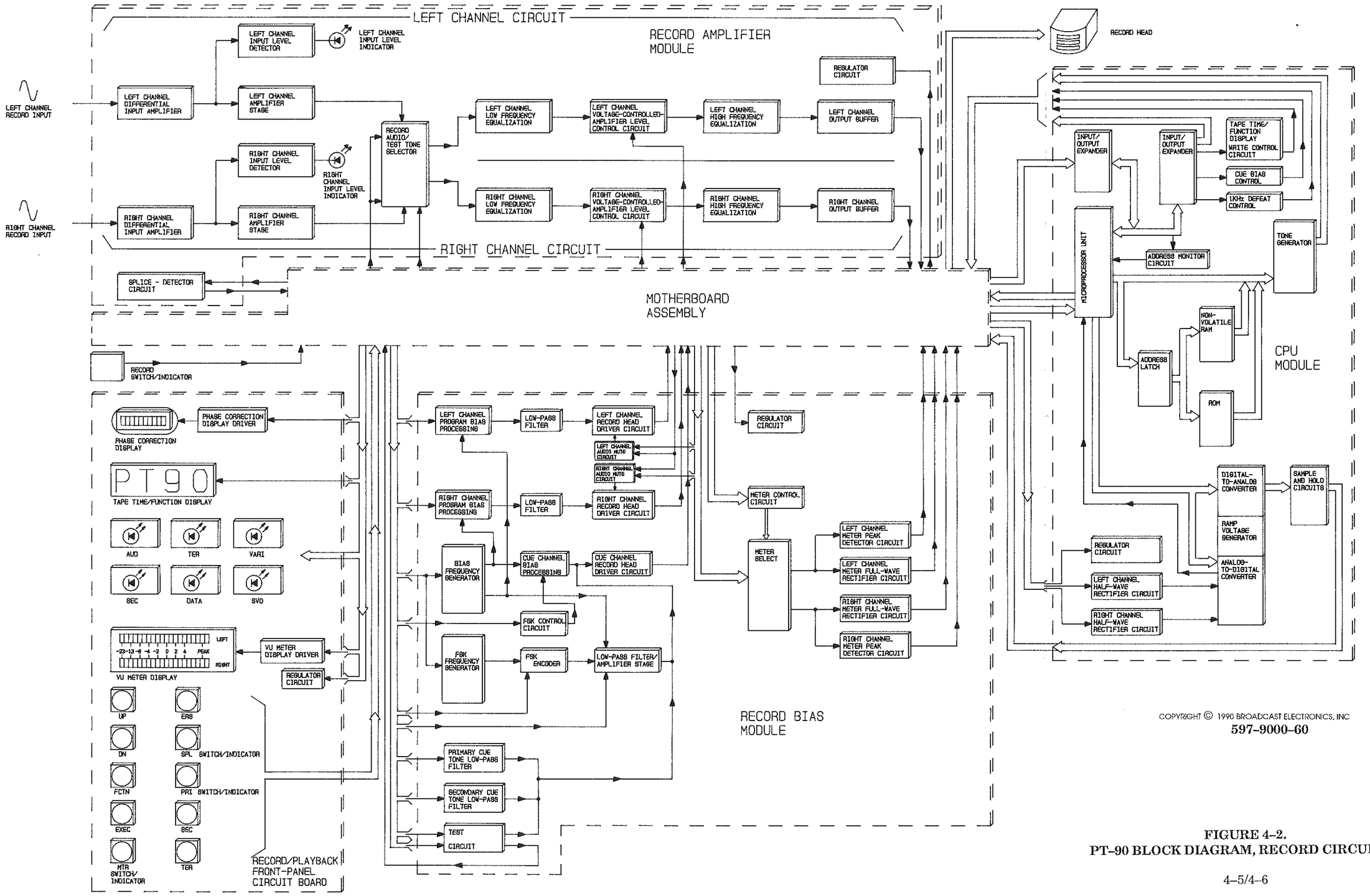

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FIGURE 4–2.
PT–90 BLOCK DIAGRAM, RECORD CIRCUITRY

4–19. The PT–90 phase correction circuitry is implemented on three hybrids: 1) left channel phase corrector, 2) right channel phase corrector, and 3) phase detector. The circuit utilizes time delay techniques to correct audio phase errors. Audio is sampled in the left channel phase corrector for use as a reference. The phase detector evaluates the sampled audio and directs the right channel phase corrector to delay the audio for the appropriate amount of time. As a result of the processing, an in–phase audio signal is generated for stereophonic or monophonic applications.

4–20. Internal circuit audio routing is provided by an audio selector. The selector routes either non–phase corrected audio, phase corrected audio, or elevated level samples for application to the audio output network. A meter amplifier circuit processes phase correction samples for application to the front panel phase correction display.

4–21. Each channel is equipped with a DYNAFEX ® noise reduction circuit. The circuit utilizes dynamically variable bandwidth limiting and a downward expander to effectively limit noise. Audio muting is provided by dual field–effect transistor networks. Solid–state output amplifier sections provide a floating electronically balanced output and short circuit protection.

4–22. **LOGIC MODULE.** All PT–90 playback operating parameters are controlled by the circuitry on the logic module. The logic module consists of individual CMOS logic gates which are organized into functional circuits. The circuits control all cartridge machine playback functions such as motor start, deck stop/start, fast forward, audio muting, and end–of–message operations. The module also contains the cue tone processing and detection circuitry.

4–23. **Start Sequence.** Cartridge machine motor operation is initiated via the motor start logic when a cartridge is inserted into the deck. Once the motor is operational, a command from the start switch/indicator will initiate a start sequence from the start logic. The start logic will energize the solenoid, illuminate the start indicators, generate an auxiliary start output, and reset the front panel tape time display via a programmable jumper.

4–24. **Stop Sequence.** Cartridge deck operation is terminated when the stop switch/indicator is depressed or when a primary cue tone is detected. The stop logic will deenergize the solenoid and extinguish the start indicators via the start logic. The stop logic will also illuminate the stop indicator and initiate start lock–out operation via the stop indicator flashing circuit.

4–25. **Fast Forward Operation.** Fast forward operation is initiated when the fast forward switch/indicator is depressed. The command will initiate fast forward operation and generate a mute command from the mute logic.

4–26. **Cue Circuit Operation.** All cue channel information is processed for application to a decoding circuit by an amplifier and equalization circuit. Cue channel decoding operations are performed by a cue filter hybrid. The hybrid will decode the applied information into primary (1 kHz), secondary (150 Hz), tertiary (8 kHz), and Frequency–Shift–Keying (FSK) signals. The outputs from the hybrid are routed to individual detector circuits.

4–27. **End–Of–Message (EOM) Operation.** An EOM circuit is incorporated into the control logic design to initiate end–of–message functions. EOM circuit operation is initiated by a secondary or tertiary cue tone detection. The EOM circuit will: 1) enable the tape time display freeze logic, 2) enable the mute logic, and 3) provide for automatic fast forward operation via a programmable jumper.

4–28. **RECORD CIRCUITRY.**

DYNAFEX ® is a registered trademark of Circuit Research Laboratories.

4–29. **FRONT PANEL CIRCUIT BOARD.** The record/playback unit phase correction display, tape time/function display, VU meter display, and 10 record function controls are housed on the front panel circuit board assembly. The front panel circuit board also contains the **AUD, SEC, DATA, TER, SVO,** and **VARI** indicators.

4–30. **MOTHERBOARD ASSEMBLY.** Internal record/playback unit communication is provided by the motherboard assembly. The motherboard assembly distributes audio and control information to the individual playback and record circuit board assemblies.

4–31. **RECORD PREAMPLIFIER MODULE.** All record input audio processing is performed by the circuitry on the record preamplifier module. The module consists of stereophonic amplifier, equalization, and control networks which process input audio for application to a record bias circuit.

4–32. Each audio channel is equipped with a differential input amplifier stage. Input level detector networks with associated indicators are incorporated into the circuit design to monitor the input audio level.

4–33. The module audio processing circuitry includes low–frequency equalization, high–frequency equalization, and VCA level control networks. Audio level control is provided by a voltage–controlled–amplifier (VCA) level control circuit. The circuit is designed with a gain of ±10 dB and provides low–noise precision control of the audio record level. High and low frequency equalization is performed by individual equalization networks. The low–frequency equalization network provides ±10 dB of low–frequency equalization. The high–frequency equalization network provides ±5 dB of high frequency equalization.

4–34. A splice–detector circuit is also incorporated into the record preamplifier module circuitry. The splice–detector circuit is designed to detect a solenoid current transient which is generated when the tape splice travels between the capstan shaft and the pressure roller. When configured for splice–find operation, the unit will operate to the fast–forward mode and automatically stop just beyond the cartridge tape splice for convenient record operation.

4–35. **RECORD BIAS MODULE.** Record bias processing, VU meter control, and cue channel processing operations are performed by circuitry on the record bias module. The module contains a record bias circuit, a frequency–shift–keying (FSK) encoder, a test tone generator, a VU meter control circuit, and primary and secondary cue tone filter networks.

4–36. **Record Bias.** The record bias circuitry consists of: 1) a precision square–wave frequency generator, 2) left and right channel program processing stages, and 3) a cue channel processing stage. Bias level control is provided by left and right channel program bias processing networks. Low–pass filter networks convert a 128 kHz square–wave bias signal to a sine–wave for application to left and right channel record head driver circuits. A cue channel bias processing circuit generates a sinusodial 128 kHz bias signal for application to the cue channel record head driver circuit.

4–37. **FSK Encoding.** RS–232 information is processed for application to the cue channel record circuit by a digital frequency–shift–keying (FSK) encoder circuit. Reference frequencies and external RS–232 information are applied to the encoder which outputs data in an FSK format. The FSK data output is applied through a low–pass filter stage for application to the cue channel record head driver circuit. An FSK control circuit is provided to enable the cue channel bias circuit.

4–38. **Test Tone Generator Circuit.** The record bias module is equipped with a test tone generator circuit. The circuit consists of a digital divider, filter network, and a control network. The circuit is controlled by a microprocessor on the CPU module and generates precision low–noise test tones for maintenance and alignment procedures. The test tone circuit also generates tertiary cue tone audio for application to the cue channel record driver circuit.

4–39. **VU Meter Control Circuit.** PT–90 record/playback unit VU meter display operations are directed by a meter control circuit. Record and playback audio information is applied to a meter select switch. A meter control circuit decodes meter switch operations and record functions to select the proper audio for application to meter rectifier and peak detector circuitry. Left and right channel full–wave rectifier and peak detector circuits process the selected audio information for application to the meter driver circuit on the front–panel circuit board assembly.

4–40. **Primary and Secondary Cue Tone Circuitry.** The record bias module also contains primary and secondary cue tone low–pass filter networks. Low–pass filter sections provide square–wave to sine–wave signal conversion of the primary and secondary cue tone audio for application to the cue channel record head driver circuit.

4–41. **CPU MODULE.** All PT–90 record operations are controlled by the CPU module. The CPU module contains an Intel 80C39 microprocessor which monitors and responds to record function commands. Digital–to–analog and analog–to–digital conversion circuitry is provided to generate internal bias, equalization, and level control commands. The module also contains a tone generator which produces primary, secondary, tertiary, and test tone signals.

4–42. **Microprocessor Control Operations.** All record function commands are interfaced to the microprocessor through an input/output expander. When a record function is initiated, the microprocessor will respond and generate the appropriate control sequence. A second input/output expander is configured for output interfacing to the tape time/function display. The input/output circuit also provides interfacing to the internal cue control and 1 kHz defeat control circuitry.

4–43. All record compensation data is stored in non–volatile RAM. The non–volatile RAM provides a stable memory environment and prevents the loss of data when ac power is removed from the unit. An address monitor circuit is incorporated into the design to provide an automatic reset command in the event of a microprocessor addressing failure.

4–44. **Digital–to–Analog and Analog–to–Digital Circuit Operation.** The microprocessor establishes record parameters by monitoring the record playback audio via an analog–to–digital circuit. Left and right channel half–wave rectifier circuits process audio samples for application to an analog–to–digital converter stage. The converter routes a digital code to the microprocessor for record parameter evaluation.

4–45. The microprocessor generates internal dc voltage levels for application to internal control circuits via a digital–to–analog converter. The converter analyzes a digital control code from the microprocessor and outputs an analog signal to sample and hold circuits for application to the bias, record level, and equalization control circuits.

4–46. **Tone Circuit.** The CPU module circuitry also contains a digital tone generator circuit. The circuit outputs primary, secondary, tertiary, and test tones as directed by the microprocessor.

4–47. FUNCTIONAL DESCRIPTION.

4–48. POWER SUPPLY MODULE.

4–49. **AC INPUT CIRCUIT.** Primary ac power is applied to the module through the ac input receptacle (refer to schematic diagram 950–0032/–001 in SECTION VII, DRAWINGS). The ac input receptacle contains built–in overload (fuse F1) and ac control (switch S201) components. Power from the receptacle is routed to the primaries of power transformer T1. The secondaries of T1 produce 20 volt and 25.6 volt ac potentials for playback circuit operations. In record/playback units, an additional 9 volt ac potential is generated for application to the record circuitry. Switch S202 provides 110V or 220V operation of the power supply circuitry.

4–50. **RECTIFIER AND FILTER CIRCUIT.** The 20 volt ac potential from transformer T1 is full–wave rectified by diodes D1 through D4 and filtered by capacitors C1 and C2 into ±22.5 volt dc supplies. The ±22.5 volt dc potentials provide operating supplies for all the PT–90 cartridge machine circuitry with the exception of the indicator lamps, the deck solenoid, and the motor.

4–51. The 25.6 volt ac potential from T1 is full–wave rectified by diodes D5 through D8 and filtered by capacitor C4 into a +28 volt dc supply. The +28 volt potential is routed to the motor, the deck solenoid, and to an indicator lamp regulator circuit consisting of transistor Q5, zener diode D15, resistor R1, and capacitor C3.

4–52. The 9 volt ac potential is full–wave rectified by diodes D9 through D12 and filtered by capacitor C5 into a +10V dc supply. The +10 volt potential is routed to the record/playback unit front–panel circuit board and logic module assemblies.

4–53. **GROUND SYSTEM.** The power supply circuit is equipped with a programmable ground system. The ground system consists of a jumper network and two ground terminals on the power supply module rear panel. The system is provided to isolate and distribute ground circuits as required for special applications. The system is shipped from the factory in a star ground configuration.

4–54. **SOLENOID DRIVER AND FOLDBACK CIRCUIT.** The solenoid driver and foldback circuit initiates and maintains solenoid operation. The circuit functions to provide a +28 volt dc operating potential to energize the solenoid, and after a specified time period, foldback the operating potential to maintain cool and efficient solenoid operation.

4–55. Before the initiation of a deck start sequence, a +28 volt potential is applied to: 1) charge an RC circuit consisting of resistor R4 and capacitor C7 and 2) bias transistor Q3 on. With Q3 on, transistor Q4 will be biased on to provide a +28 volt potential for initial solenoid operation. +12 volt regulator IC–1 is temporarily isolated from the circuit. Potentiometer R9 provides calibration of the solenoid foldback current..

4–56. When a deck start sequence is initiated, a HIGH from the solenoid start circuit on the logic module will bias driver transistor Q1 on. Q1 will bias transistor Q2 on to energize the solenoid. With Q2 on, RC circuit R4 and C7 will discharge. After approximately 100 milliseconds, transistor Q3 will be biased off which disables transistor Q4. With Q4 off, the +28 volt potential is routed through regulator IC–1 to maintain a constant current source of 0.325 amperes at approximately +12V for continuous solenoid operation.

4–57. **MOTOR CONTROL CIRCUIT BOARD.**

4–58. **REFERENCE CIRCUIT.** A precision reference signal for servo circuit operation is generated by a 460.8 kHz crystal controlled oscillator circuit consisting of crystal Y1, capacitors C30, C31, and resistor R54 (refer to Figure 4–3). The oscillator circuit output is applied to divider U11.

4–59. Divider U11 is designed to generate motor frequency references. The output of U11 and motor speed jumper network W1 is applied to divide–by–three stage U12A/B. The output of divider U12A/B is routed to multiplexer network U13A/B. U13A/B is designed to switch between normal and fast forward motor frequency references. Jumper network W3 provides input information for the multiplexer network. The output of multiplexer U13A/B is routed for application to a frequency comparator circuit. The following is list provides motor reference frequencies and corresponding motor speeds.

MOTOR REFERENCE FREQUENCY (Hz)		MOTOR SPEED (Inches–Per–Second)	
NORMAL	FAST FORWARD	NORMAL	FAST FORWARD
1200	3600	15	—
600	1800	7.5	22.5
300	900	3.75	11.25

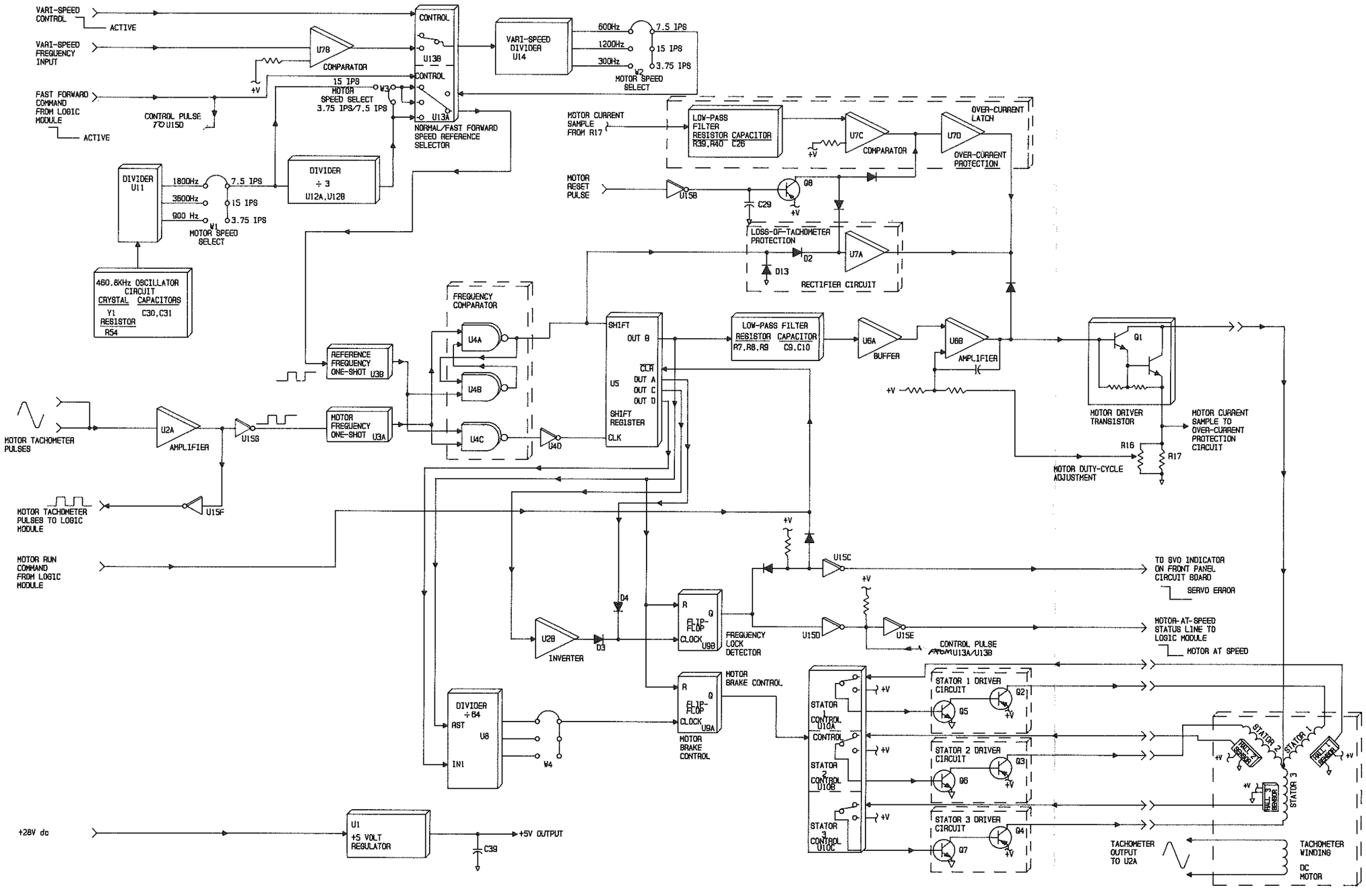

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FIGURE 4-3. MOTOR CONTROL CIRCUIT BOARD SIMPLIFIED SCHEMATIC

4–60. **Normal/Fast Forward Operation.** With the unit in the normal mode and programmed for 7.5 IPS operation, divider U11 will output an 1800 Hz reference to divider U12A/B and multiplexer U13A/B via jumper network W3. U12A/U12B will output a 600 Hz reference to multiplexer U13A/B. The vari–speed and fast forward control lines will be HIGH to instruct multiplexer U13A/B to output a 600 Hz motor reference frequency for application to a frequency comparator circuit.

4–61. When the unit is operated to the fast forward mode, the fast forward control line will go LOW. The LOW instructs multiplexer U13A/B to output an 1800 Hz reference for application to a frequency comparator circuit.

4–62. **TACHOMETER PROCESSING CIRCUIT.** An indication of cartridge machine motor speed is generated by a tachometer winding. When the unit is programmed for 7.5 IPS operation and the motor is at full speed, the tachometer will output a sinusoidal 600 Hz signal to high gain amplifier stage U2A. U2A is configured for a gain of approximately 1000. The output of U2A is applied to inverters U15F and U15G. U15F generates square–wave tachometer pulses for application to the logic module. U15G generates square–wave tachometer pulses for application to a frequency comparator circuit.

4–63. **FREQUENCY COMPARATOR CIRCUIT.** The frequency comparator circuit consists of a one–shot network, a frequency comparator, and a shift register. The one–shot network consists of integrated circuits U3A/B. The reference circuit output (600 Hz for 7.5 IPS operation) is applied to one–shot U3B. The motor tachometer reference is applied to one–shot U3A. The one–shots are designed to generate precision square–wave signals for application to the frequency comparator.

4–64. The frequency comparator network consists of NAND gates U4A/B/C. The circuit functions to compare the applied frequencies and generate corresponding shift and clock signals to shift register U5 and a rectifier network. Shift register U5 will generate four outputs which represent operating parameters such as motor load and speed. The outputs provide information for a motor driver circuit, a motor brake control circuit, and a motor protection circuit.

4–65. **MOTOR DRIVER CIRCUIT.** One output from shift register U5 is filtered into a dc level by a passive low–pass filter consisting of resistors R7, R8, R9 and capacitors C9 and C10. The dc level is buffered by operational amplifier U6A and applied to amplifier stage U6B. U6B will output a varying bias voltage to motor driver transistor Q1. Q1 is designed to provide a dc supply voltage which controls the speed of the motor. Potentiometer R16 provides motor drive calibration.

4–66. **MOTOR PROTECTION CIRCUIT.** The motor is monitored for loss of tachometer signals and over–current conditions by a protection circuit. A rectifier circuit consisting of diodes D2 and D13 and operational amplifier U7A function as a tachometer monitor network. With the application of tachometer signals, the output of U7A will be HIGH to allow normal motor drive operation. With the loss of tachometer pulses, the output of U7A will go LOW to bias Q1 off and terminate motor operation.

4–67. Motor over–current conditions are monitored by a circuit consisting of a passive low pass filter, comparator U7C, and latch U7D. A motor current sample is filtered into a dc level by a low–pass filter consisting of resistors R39, R40, and capacitor C26. The dc signal is applied to comparator U7C and latch U7D. When the motor current sample is below the reference level at U7C, U7C will output a HIGH to latch U7D. U7D will output a HIGH to allow normal motor drive operation. When the motor current sample increases above the comparator reference level, U7C will output a LOW to latch U7D. U7D will output a LOW to bias Q1 off and terminate motor operation. A timing circuit consisting of inverter U15B, transistor Q8, and capacitor C29 functions to disable the over–current protection circuit for approximately 3 seconds during initial motor operation.

4–68. **MOTOR LOCK DETECTOR CIRCUIT.** Samples from U5 are monitored for motor unlocked conditions by inverter U2B, diode D4, and flip–flop U9B. When the motor is operating in a locked condition, a HIGH is applied to inverter U2B and a LOW to diode D4. U2B will output a LOW to frequency lock detector flip–flop U9B. The output of U9B will go LOW. The LOW is routed through inverters U15D and U15E to output a LOW to indicate a motor–at–speed condition. When an unlocked motor condition occurs, the output of U2B will go HIGH or diode D4 will conduct to generate a clock pulse for flip–flop U9B. The output of U9B will go HIGH. Inverter U15C will output a LOW to illuminate the front panel **SVO** indicator. The HIGH from U9B is also applied through inverters U15D and U15E to indicate an unlocked motor condition.

4–69. **MOTOR COMMUTATOR CONTROL CIRCUIT.** The motor commutator control circuit consists of a stator control/driver network and a brake control circuit. Multiplexer U10A/B/C and transistors Q2 through Q7 operate together to control the direction of the motor stators. Divider U8 and motor brake control flip–flop U9A initiate motor braking operations when: 1) the motor is operating at a fast forward rate and required to return to the normal operating speed and 2) at motor termination.

4–70. When the motor is in normal or fast forward operation, output samples from U5 will force the output of divider U8 LOW. The LOW is applied to motor brake control flip–flop U9A. The output of U9A will go LOW. With the output of U9A LOW, stator control logic U10A/B/C and the transistor driver circuits operate individually to control each motor stator. A signal from hall effect sensor 1 will be routed through stator control device U10A to the stator 1 driver circuit. The driver circuit will output the signal to control the operation of stator 1. Stator 2 and 3 control/driver networks operate in an identical manner. The stator control/driver circuitry will respond in the appropriate sequence to initiate and control motor commutator rotation.

4–71. When a motor braking operation is required, the motor drive samples from U5 will produce a square–wave clock signal from U8. The clock signal is applied to flip–flop U9A which outputs a corresponding square–wave control signal to the stator control logic. The stator control logic will respond by simultaneously applying a +28 volt pulse to each stator to provide a motor braking action. When the motor returns to a locked condition, the output of U9A will go LOW to terminate motor braking operation and provide normal stator control.

4–72. **VARI–SPEED CIRCUIT.** The cartridge machine motor may be varied a minimum ±10% for special audio applications by a vari–speed feature. The vari–speed circuitry consists of comparator U7B, divider U14, and jumper network U2. The circuit operates from a nominal 9600 Hz external signal source.

4–73. The vari–speed signal source is applied to comparator U7B. U7B is designed to generate a square–wave reference signal for application to multiplexer U13B. When a LOW is applied to the vari–speed control line, multiplexer U13B will route the reference signal to divider U14. U14 will output a corresponding reference signal for application to U13A and the reference circuitry.

4–74. **POWER SUPPLY CIRCUIT.** The motor control circuit board power supply circuit consists of regulator U1 and capacitor C39. U1 and capacitor C39 regulate the +28V dc voltage into a +5 volt supply for circuit operations.

4–75. **AUDIO MODULE.**

4–76. The following text describes the operation of the audio module. Stereophonic units are equipped with left and right channel audio circuits and automatic phase correction circuitry. Monophonic units are equipped with only the left channel audio circuit. The left and right channel audio circuits are identical; therefore, only the left channel circuit will be discussed.

4–77. A simplified schematic diagram of the audio module is presented in Figure 4–4. Refer to Figure 4–4 as required for the following circuit description.

4–78. **AUDIO INPUT CIRCUIT.** Left channel audio from the tape head is applied to operational amplifier U1. U1 is configured as an audio amplifier and equalization stage with a gain of approximately 50 dB. Potentiometer R11 provides ±6 dB of low frequency equalization. Potentiometer R6 provides ±10 dB of high frequency equalization. The output of amplifier/equalization stage U1 is applied to the automatic phase correction circuit.

4–79. **AUTOMATIC PHASE CORRECTION CIRCUIT.** The automatic phase correction circuitry is implemented on three hybrid circuits: 1) left channel phase corrector PC–2, 2) right channel phase corrector PC–3, and 3) phase detector PC–1. The circuit is designed to continuously monitor left and right channel audio and automatically correct phase errors to produce in–phase audio.

4–80. The phase correction circuitry utilizes time delay techniques to correct audio phase errors. Left channel audio is applied to phase corrector PC–2 which contains a fixed time delay segment. The audio at PC–2 is sampled and used as reference by phase detector PC–1. Phase detector PC–1 evaluates the left channel audio sample and outputs a control oscillator signal to right channel corrector PC–3. PC–3 contains a variable time delay segment which delays the right channel audio from 0.8 to 1.2 milliseconds as directed by the oscillator signal from PC–1. As a result of the processing, an in–phase audio signal is produced for application to an audio selection circuit.

4–81. Phase correction calibration is provided by potentiometer R35. A sample from phase detector PC–1 is used for phase correction display applications. The sample is applied to U3B which is configured as a differential amplifier. U3B outputs a varying control voltage to drive the front panel phase correction display.

4–82. **AUDIO SELECTION CIRCUIT.** Integrated circuit U4 operates as an audio selector. U4 is designed to select one of the following types of audio as determined by phase correction circuit programming and elevated level comparator U3A. Resistors R32, R33, R36, and R37 attenuate elevated level signal to generate the appropriate audio level. The output of selector U4 is routed for application to the noise reduction circuit.

AUDIO TYPE

1. Non–phase corrected audio.
2. Phase corrected audio.
3. Elevated level non–phase corrected audio.
4. Elevated level phase corrected audio.

4–83. Elevated level comparator U3A and phase correction enable/disable jumper J402 control the operation of audio selector U4. Elevated level operation is initiated when the deck elevated level sensor outputs a control signal to comparator U3A. The output of U3A will go HIGH to configure U4 for elevated level audio. The phase correction circuit may be disabled at U4 by installing jumper J402 in the appropriate position.

4–84. **NOISE REDUCTION CIRCUIT.** The noise reduction circuit incorporates dynamic variable bandwidth limiting and a downward expansion technique to effectively reduce the noise level. The operational noise reduction circuitry is housed on integrated circuit U11. Operational amplifier U10A is configured as a high–pass filter/amplifier stage which controls the circuit sensitivity. The output of U11 is applied through U10B which operates as a current–to–voltage converter.

4–85. **MUTE CIRCUIT.** The noise reduction circuit output is applied to an audio mute circuit. The mute circuit consists of a control device and shunt–series field–effect–transistor network. When audio muting is required, a LOW is applied to mute control transistor Q3 and left channel mute transistor Q4. The LOW is inverted by transistor Q3 which routes a HIGH to transistor Q1. The LOW will bias Q4 on and the HIGH will bias Q1 off to mute the applied audio signal.

4–86. **OUTPUT AMPLIFIER CIRCUIT.** Audio from the mute circuit is applied to U5A which is configured as an amplifier stage. Potentiometer R40 provides left channel output level control. The output of U5A is applied to the left channel output amplifier network consisting of inverter U6A and amplifier stages U7A/B and U6B. The amplifier network is configured for a gain of two. The unique operation of the network provides a balanced or unbalanced output without loss of audio signal.

4–87. Audio from U5A is routed through inverter U6A and applied to the amplifier stage in an inverted and non–inverted format. Inverted audio is applied to amplifier stage U7A. Non–inverted audio is applied to amplifier stage U7B. Together, U7A and U7B operate as a balanced audio output amplifier stage with a gain of two. Amplifier U6B functions as a monitoring and gain stage for a shorted audio output condition.

4–88. When the audio output impedance is balanced, the input to U6B is at virtual ground which isolates the stage from the circuit. When either the positive or negative output terminals are grounded, an audio signal will be applied to U6B. U6B will output a signal to increase the gain of the remaining amplifier network operating stage. As a result, the network will output a full signal into the unbalanced output condition.

4–89. **POWER SUPPLY CIRCUIT.** The module power supply circuit consists of a positive and negative regulator and filter network. A +22 volt dc supply from the power supply module is regulated into a +16.5 volt potential by regulator U13 and capacitor C61. The +16.5 volt supply is re–regulated into a +8 volt supply by regulator U15 and capacitor C88.

4–90. A –22.0 volt potential from the power supply module is regulated into a –16.5 volt dc potential by regulator U14 and capacitor C62. The –16.5 volt potential is re–regulated into a –8 volt dc supply by regulator U16 and capacitor C89.

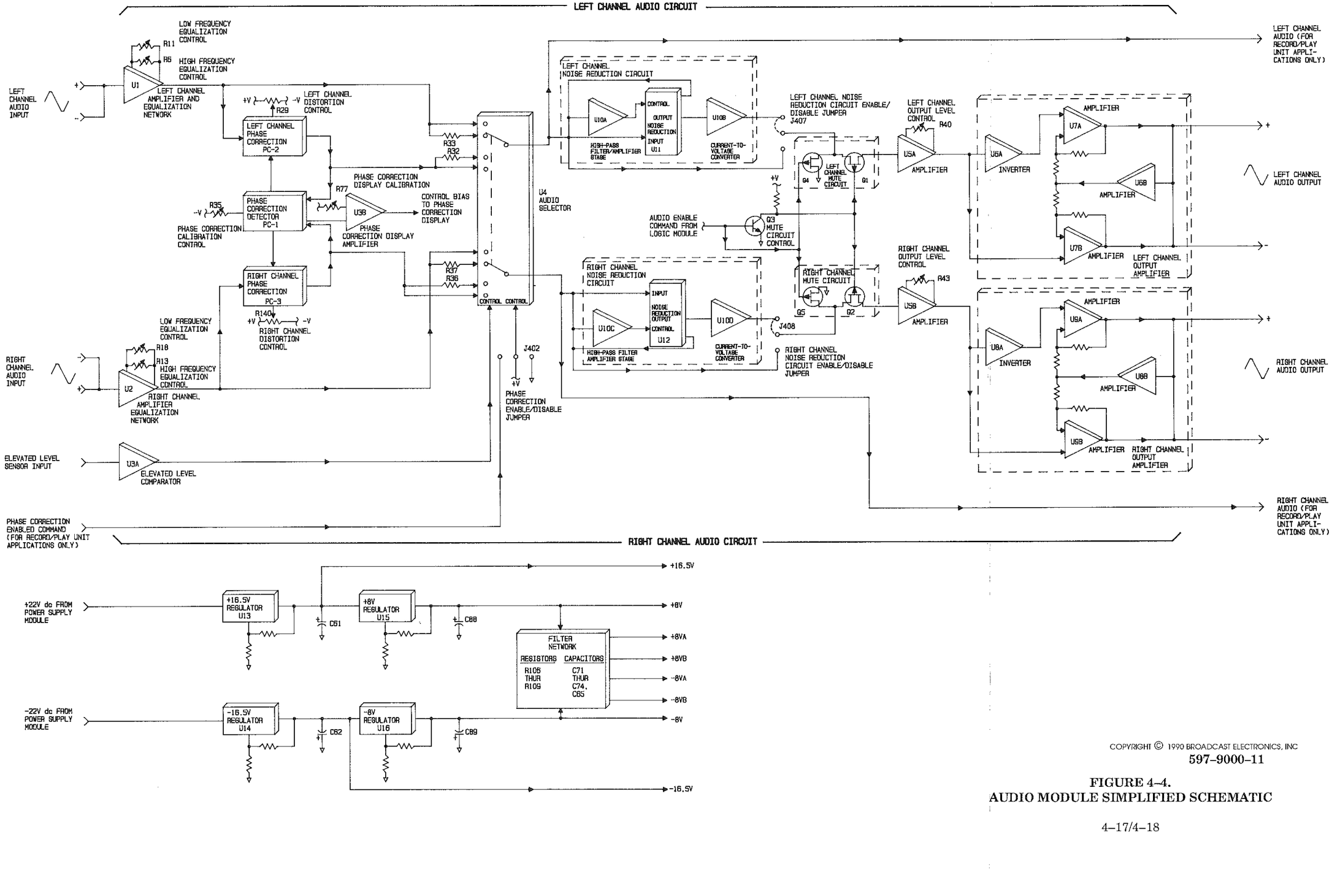
4–91. The ±8 volt potentials are routed to a special RC filter network. The network provides additional filtering for the phase correction circuit.

4–92. **LOGIC MODULE.**

4–93. All cartridge machine playback operating parameters are controlled by the logic module (refer to Figure 4–5). The module design utilizes individual CMOS logic components. The logic gates are organized into circuits which control motor and solenoid operations, deck stop/start operations, fast forward operation, audio muting, end–of–message functions, and operating indicators.

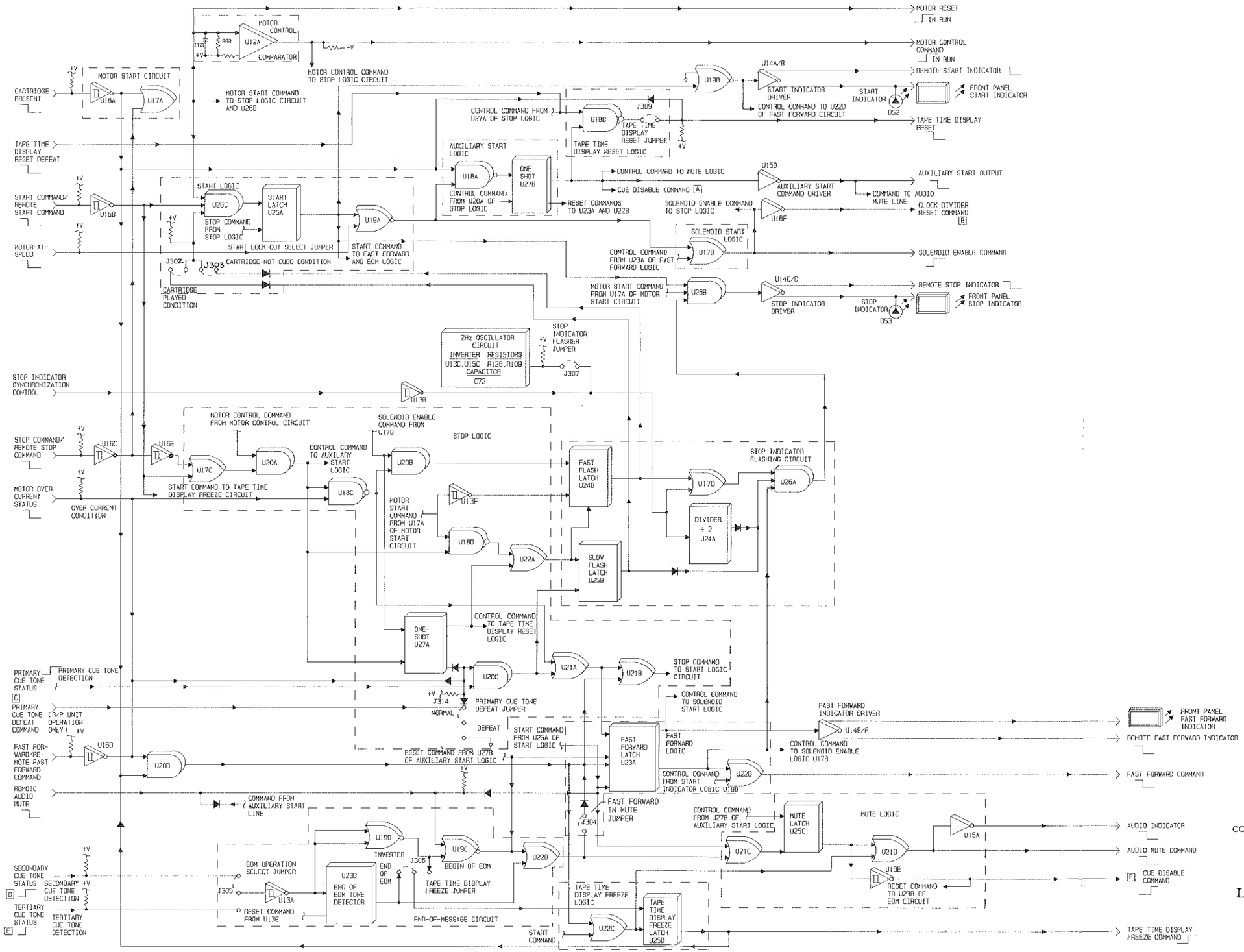
4–94. **MOTOR CONTROL LOGIC.** Motor operations are directed by the motor start and control circuits. A normal cartridge machine motor start sequence is initiated when a cartridge is inserted into the deck. A LOW from the deck micro–switch is applied to a motor start circuit consisting of inverter U16A and OR gate U17A. U17A gates a HIGH from U16A and a LOW from inverter U16C to output a continuous HIGH motor start command to the motor control circuit, the start logic, and the stop logic.

4–95. The motor control logic consists of comparator U12A and an RC timing circuit. U12A is designed to control motor operations in response to a normal or maintenance mode start sequence. With the initiation of a normal start sequence, the continuous HIGH from U7A will be above the reference at U12A. The output of U12A will go HIGH to initiate motor operation. When the cartridge is removed, RC circuit R99 and C68 will begin to discharge. After approximately 90 seconds, U12A will output a LOW to terminate motor operation.



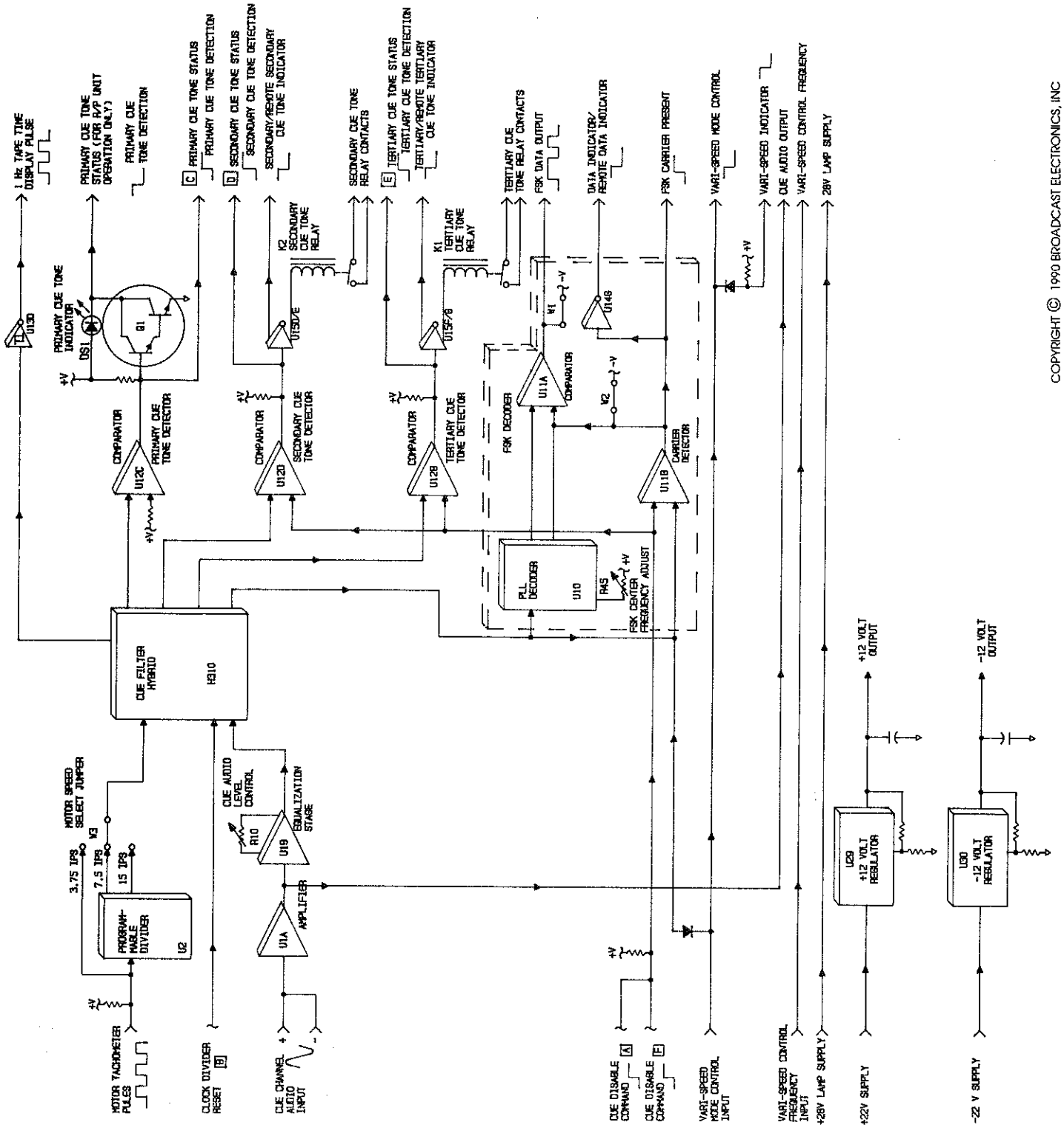
597-9000-11

FIGURE 4–4.
AUDIO MODULE SIMPLIFIED SCHEMATIC



597-9000-12A

FIGURE 4–5.
LOGIC MODULE SIMPLIFIED SCHEMATIC (Sheet 1 of 2)



597-9000-12B

FIGURE 4–5. LOGIC MODULE SIMPLIFIED SCHEMATIC
(Sheet 2 of 2)

4–96. **Maintenance Mode Operation.** The motor control circuit also responds to a maintenance mode start sequence. A maintenance mode motor start command is generated when a cartridge is removed from the deck and the stop switch/indicator is momentarily depressed. OR gate U17A will output a momentary HIGH to charge RC circuit R99 and C68. With the voltage from the RC circuit above the reference at U12A, the output of U12A will go HIGH to start the motor. After approximately 90 seconds, the RC circuit will completely discharge. The output of U12A will go LOW to terminate motor operation.

4–97. **DECK START LOGIC.** A deck start sequence is initiated when the front–panel **START** switch/indicator is depressed. A LOW from the switch/indicator is inverted by U16B and routed to the start logic, stop logic, and the tape time display freeze circuit.

4–98. The deck start logic consists of AND gate U26C, latch U25A, and NOR gate U19A. U26C gates HIGH control commands from the motor start circuit, inverter U16B, and start lock–out select jumper J303. The output of U26C will go HIGH to reset start latch U25A. U25A will output a LOW to start indicator driver network U19B and U14A/B. U14A/B will output a LOW to illuminate start indicator DS2 and the local/remote start indicators. The LOW from U25A is also routed to: 1) NOR gate U19A, 2) the stop indicator driver network, 3) the fast forward logic, and 4) the mute circuit. U19A gates a LOW from start latch U25A and a LOW from the motor–at–speed control line to output a HIGH to the auxiliary start logic and to the solenoid start circuit.

4–99. **Solenoid Start Logic.** OR gate U17B functions as the solenoid start logic. U17B gates a HIGH command from U19A of the start logic and LOW from the fast forward logic. The output of U17B will go HIGH to enable the solenoid driver circuit.

4–100. **Auxiliary Start Logic.** NAND gate U18A and one–shot U27B are configured as the auxiliary start logic. An auxiliary start command sequence is initiated when U18A gates HIGH logic commands from U19A and U16A. The output of U18A will go LOW to trigger one–shot U27B. U27B will output a HIGH through inverter U15B to generate a LOW auxiliary start command. U27B also routes HIGH logic commands to the tape time display reset logic, cue filter circuit, and the mute logic. LOW reset commands from U27B are routed to the fast forward logic and the EOM circuit.

4–101. **DECK STOP LOGIC.** The deck stop logic consists of a stop circuit and a stop indicator flashing circuit. Together, the circuits are responsible for generating deck stop commands, start lock–out commands, and stop indicator control.

4–102. **Deck Stop Operation, Manual.** When deck operation is terminated manually, a LOW from the front–panel **STOP** switch/indicator is applied through inverters U16C and U16E to OR gate U17C. U17C gates LOW logic commands from U16E and U16B to output a LOW to U20A. U20A gates the LOW from U17C and a HIGH motor start command from U12A to output a LOW to reset the auxiliary start logic. U20A also routes a LOW to NAND gates U18C and U18D and one–shot U27A. U18C is designed to monitor the motor over–current status line. With normal motor current conditions, U18C will gate a HIGH from the status line and the LOW from U20A to output a HIGH to AND gate U20B and OR gate U21A.

4–103. With the LOW command from U20A, one–shot U27A will output both HIGH and LOW logic commands. HIGH logic commands are routed to OR gate U22A and the tape time display reset logic. A LOW is applied to AND gate U20C which monitors the primary cue tone status line. U20C will output a LOW to OR gate U21A and to the stop indicator flashing circuit. U21A gates a LOW from U20C and a HIGH from U18C to output a HIGH to OR gate U21B. U21B gates the HIGH from U21A and a LOW from U20D to route a HIGH stop command to reset the start logic. U25A of the start logic will output a LOW to extinguish the start indicator via U19B and U14A/B. U19A of the start logic will deenergize the solenoid via U17B. The stop indicator will illuminate as directed by a stop control circuit and the stop indicator flashing circuit.

4–104. **Deck Stop Operation, Primary Cue Tone.** When a primary (1 kHz) cue tone is detected, the primary cue tone status line will go HIGH. U20C gates HIGH logic commands from the primary cue tone status line and one–shot U27A to output a HIGH through OR gate U21A to OR gate U21B. U21B will output a HIGH to reset the start logic. With the start logic reset, U25A will output a LOW to extinguish the start indicator and deenergize the solenoid. The stop indicator will illuminate as directed by a stop control circuit and the stop indicator flashing circuit. Jumper J314 is incorporated into the logic to disable primary cue tone operation.

4–105. **Stop Indicator Control Logic.** The cartridge machine deck stop indicator is designed to provide indications of special operations. Control commands for stop indicator operation are generated by logic gates U20B, U13F, U18D, and U22A of the stop circuit. The control commands are processed through the stop indicator flashing circuit consisting of latches U24B and U25B, divider U24A, OR gate U17D, AND gate U26A to generate the appropriate indicator response.

4–106. When deck operation is terminated by the local or remote stop switch/indicator, U20B gates a HIGH solenoid enable command from U17B and a HIGH from NAND gate U18C. U20B will route a HIGH to set fast flash latch U24B. The output of U24B will go LOW. U22A gates HIGH logic commands from NAND gate U18D and one–shot U27A to output a HIGH to set slow flash latch U25B. With the output of latch U24B LOW and the stop indicator flashing oscillator circuit disabled at jumper J307, a HIGH from U13B is routed through U17D to AND gate U26A. U26A gates HIGH control commands from U17D, slow flash latch U25B, and fast forward latch U23A to output a HIGH to AND gate U26B. U26B gates HIGH logic commands from U26A, U17A, and start latch U25A. U26B will output a HIGH through inverter U14C/D to illuminate stop indicator DS3, the front panel stop indicator, and the remote stop indicator.

4–107. **Stop Indicator Flashing/Start Lock–out Operation.** Stop indicator flashing is enabled when jumper J307 is installed. A two Hz reference signal from an oscillator circuit consisting of inverters U13C, U15C, resistors R126, R109, and capacitor C72 is routed to divider U24A and OR gate U17D. When deck operation is terminated by the local or remote stop switch/indicator, U20B will gate a HIGH solenoid enable command and a HIGH command from U18C to output a HIGH to set latch U24B. U24B will output a LOW to start lock–out jumper J303 and to OR gate U17D. The LOW will initiate start lock–out operation for a cartridge–not–cued condition if jumper J303 is installed. With one input to U17D LOW, the two Hz pulse from the oscillator circuit is routed to U26A. With HIGH commands from U25B and U23A, U26A will route the oscillator signals to U26B to generate a two Hz stop indicator flashing rate for a cartridge–not–cued condition.

4–108. If deck operation is terminated by a primary cue tone detection, HIGH logic commands from latch U27A and the primary cue tone status line are gated at U20C. U20C will output a HIGH to reset slow flash latch U25B. U25B will output a LOW to start lock–out jumper J302. The LOW will initiate start lock–out operation for a cartridge played condition if start lock–out jumper J302 is installed.

4–109. An indication of the primary cue tone detection is generated by the oscillator circuit and the operation of divider U24A, OR gate U17D, and AND gate U26A. The two Hz pulses from the oscillator circuit are routed through divider U24A to generate a one Hz pulse. With the output of U25B HIGH, U26A gates HIGH commands from U17D and U23A and the one Hz pulses from U24A. U26A will output the oscillator pulses through U26B to generate a one Hz stop indicator flashing rate for a cartridge played condition.

4–110. Stop indicator flashing and start lock–out operations are reset when the local/remote stop switch/indicator is depressed or when the cartridge is removed. U20B will gate a LOW solenoid enable command and a HIGH from U18C to output a LOW to latch U24B. U18D will gate a HIGH motor start command and a LOW from U20A to output a HIGH to OR gate U22A. U22A will output a HIGH clock pulse to reset latch U24B and set latch U25B. The outputs of U24B and U25B will go HIGH to reset the stop indicator flashing and start lock–out operation.

4–111. **FAST FORWARD LOGIC.** When the fast forward switch/indicator is depressed, a LOW is applied through inverter U16D to AND gate U20D. U20D gates HIGH logic commands from U16D and U16A to output a HIGH to fast forward latch U23A, the tape time display freeze logic, and to U21B of the stop logic. U21B will output a HIGH to reset the start logic. The start logic will extinguish the start indicator and output a LOW to solenoid start logic U17B. The tape time display freeze logic will enable tape time display and output a LOW to U21D of the mute logic. The output of U21D will go LOW to enable the audio mute circuit on the audio module.

4–112. Fast forward latch U23A will respond by generating both HIGH and LOW logic commands. A HIGH logic command will be routed to the solenoid start logic to maintain solenoid operation. A HIGH is also routed through inverter U14E/F to illuminate the local and remote fast forward indicators. A LOW logic command is applied to OR gate U22D. U22D gates a LOW from U23A and a LOW from the start logic to output a LOW fast forward command to the motor control circuit board. A LOW is also applied to the stop indicator flashing circuit to extinguish the stop indicator. Jumper J304 provides automatic fast forward operation during audio mute conditions.

4–113. **END–OF–MESSAGE (EOM) LOGIC.** The EOM circuit is designed to initiate a variety of control operations at the end of a tape cartridge message. The EOM circuit consists of four logic gates and a end–of–tone detector.

4–114. EOM circuit operation is initiated by a secondary or tertiary cue tone. Jumper J305 dedicates either the secondary or tertiary cue tone for EOM operation. When the selected cue tone is detected, a HIGH is applied through jumper J305 to inverter U13A. U13A will output a LOW to inverter U19D and to end–of–tone detector U23B. U19C gates a HIGH from U19D and a HIGH from the remote audio mute line to output a LOW to OR gate U22B. At the end of the pulse from U13A, end–of–tone detector U23B will output a HIGH to tape time display freeze jumper J306 and to U22B. J306 determines if the tape time display is frozen at the beginning or the end of the EOM tone. U22B gates a HIGH from U23B and a LOW from U19C to output a HIGH to U21C to enable the mute logic.

4–115. **TAPE TIME DISPLAY FREEZE LOGIC.** The tape time display freeze logic consists of OR gate U22C and latch U25D. At the beginning or end of the EOM tone, the EOM circuit will output a HIGH to tape time display freeze latch U25D. U25D will output a HIGH to freeze the tape time display. When the fast forward or start switch/indicators are depressed, U22C will route a HIGH to latch U25D. U25D will respond by routing a LOW to enable the tape time display.

4–116. **TAPE TIME DISPLAY RESET LOGIC.** The tape time display reset logic consists of NAND gate U18B and jumper J309. The logic will output a LOW to reset the tape time display on start commands.

4–117. **MUTE LOGIC.** The mute logic controls the operation of the muting circuits on the audio module. When the end of a message is detected by the EOM circuit or when the remote audio mute command goes LOW, U21C will output a HIGH to mute latch U25C. The output of U25C will go LOW. U21D gates a LOW from U25C and a LOW from the tape time display logic to output a LOW audio mute command. The LOW from U21D is inverted by U15A to extinguish the front–panel audio indicator. A LOW from U25C is also applied through inverter U13E to provide a HIGH disable command to the cue circuitry.

4–118. **CUE CIRCUIT.** The cue circuit is designed to amplify and decode all cue channel information. The cue circuit consists of: 1) a preamplifier and equalization stage, 2) a cue filter hybrid, 3) individual primary, secondary, and tertiary cue tone detectors, and 4) an FSK decoder.

4–119. **Cue Audio Amplifier Circuit.** Cue audio information from the tape head is applied to amplifier stage U1A. U1A is configured for a gain of approximately 30 dB. The output of amplifier U1A is routed to operational amplifier U1B which is configured as an equalization stage. Potentiometer R10 provides cue audio level control. The output of U1B is routed for application to the cue filter hybrid.

4–120. **Cue Filter Hybrid.** All cue channel information is processed by cue filter hybrid H310. H310 consists of a reference processing circuit and individual 1 kHz, 3.5 kHz, 8 kHz and 150 Hz bandpass filters. The hybrid will filter all applied primary, secondary, and tertiary cue tone information into corresponding dc levels for application to the detector circuits. FSK information is filtered and routed to the FSK decoder. The hybrid also generates one Hz reference pulses for application to the tape time display.

4–121. A reference for cue filter hybrid H310 is provided by programmable divider U2. Motor tachometer pulses are routed through divider U2 and motor speed select jumper W3 to output a constant 300 Hz reference for cue filter operations.

4–122. **Primary, Secondary, And Tertiary Comparator Circuits.** Primary, secondary, and tertiary cue tone information from cue filter hybrid H310 is routed to primary cue tone comparator U12C, secondary cue tone comparator U12D, and tertiary cue tone comparator U12B. When the primary cue tone output from H310 increases above the reference at U12C, the output of comparator U12C will go HIGH. The HIGH is applied to the primary cue tone status line and will illuminate primary indicator DS1 by enabling transistor Q1.

4–123. When the secondary cue tone output from H310 increases above the reference at U12D, the output of comparator U12D will go HIGH. The HIGH is applied to the secondary cue tone status line and to inverter U15D/E. U15D/E will output a LOW to illuminate the local and remote indicators and to energize secondary cue tone relay K2. Tertiary cue tone comparator U12B operates in an identical manner.

4–124. **Frequency–Shift–Keying (FSK) Decoder Circuit.** The FSK decoder consists of PLL decoder U10, comparator U11A, and detector U11B. FSK information is binary data which frequency modulates a carrier. In broadcast applications, the carrier frequency is 3500 Hz. Binary 1 data will shift the carrier to 3650 Hz (space frequency). Binary 0 data will shift the carrier to 3350 Hz (mark frequency).

4–125. The FSK information from cue filter hybrid H310 is applied to PLL decoder U10 and carrier detector U11B. Decoder U10 locks to the FSK carrier frequency and generates a corresponding dc output as the carrier shifts to the mark and space frequencies. The output of decoder U10 is applied to comparator U11A which processes the data into an RS–232 format. Potentiometer R45 provides FSK decoder circuit center frequency calibration. The decoder circuit will be disabled if the unit is operated in the vari–speed mode, fast forward, or when the audio is muted.

4–126. Operational amplifier U11B operates as a carrier detector. If information from cue filter hybrid H310 is present, U11B will output a HIGH to the carrier present status line. The HIGH is also inverted at U14G to illuminate the local and remote data indicator.

4–127. **POWER SUPPLY.** Operating potentials for logic module components are generated by a voltage regulator circuit. A +22V supply is regulated into a +12 volt dc operating potential by regulator U29. A –22V supply is regulated into a –12 volt dc potential by regulator U30.

4–128. **MOTHERBOARD ASSEMBLIES.**

4–129. The PT–90 series motherboards provide all cartridge machine internal circuit communication. The motherboard assemblies distribute audio, power, and control signals for application to the circuit board assemblies.

4–130. **PLAYBACK UNIT FRONT PANEL DISPLAY CIRCUIT BOARD.**

4–131. The playback unit front panel display circuit board contains the phase correction display, the tape time display, and the AUD, SEC, TER, DATA, VARI, and SVO indicators (refer to schematic diagram SC910–9003–1 in SECTION VII, DRAWINGS). The circuit board also contains the associated display driver and control networks.

4–132. **PHASE CORRECTION DISPLAY.** A varying dc control voltage input from the phase correction display driver circuit on the audio module is applied to integrated circuit U1. U1 is a dot/bar display driver which controls the operation of phase correction display DS7. DS7 is a ten–segment multi–color LED display operated in a moving bar format. Driver U1 evaluates the applied input voltage and illuminates the correct segments of the display to provide a relative indication of audio phase correction.

4–133. **TAPE TIME DISPLAY.** The tape time display is controlled by logic circuitry on the logic module. Tape time display freeze/count control, one Hz reference signals, and reset control information is applied to integrated circuit U2. U2 is a four–digit up/down counter and display driver. U2 processes the applied control information and generates the appropriate output commands to operate four digit seven segment tape time display DS8.

4–134. **AUD, SEC, TER, DATA, VARI, AND SVO INDICATORS.** The **AUD, SEC, TER, DATA, VARI,** and **SVO** indicators provide status information on various cartridge machine operating parameters. LOW control commands from the logic circuit board will be applied to illuminate the appropriate indicator as required. The following list presents a description and reference designator of each indicator.

INDICATOR	REFERENCE DESIGNATOR	DESCRIPTION
AUD	DS1	AUDIO INDICATOR
SEC	DS2	SECONDARY CUE TONE INDICATOR
TER	DS3	TERTIARY CUE TONE INDICATOR
DATA	DS4	DATA INDICATOR
VARI	DS5	VARI–SPEED MODE INDICATOR
SVO	DS6	SERVO MOTOR INDICATOR

4–135. **RECORD/PLAYBACK UNIT FRONT PANEL DISPLAY CIRCUIT BOARD.**

4–136. The record/playback unit function switches, the phase correction display, the VU meter display, the tape time/function display, and the indicator circuitry are housed on the front panel display circuit board (refer to schematic diagram SD910–9011 in SECTION VII, DRAWINGS). The circuit board also contains the associated phase correction and VU meter display driver circuitry.

4–137. **PHASE CORRECTION DISPLAY.** The phase correction display is controlled by a varying dc voltage input from the phase correction display driver on the audio module. The control voltage is applied to dot/bar display driver U1. U1 evaluates the applied input voltage and generates the appropriate control sequence to illuminate the appropriate segments of phase correction display DS7. DS7 is a multi–color ten segment LED display operated in a moving bar format. The display provides the operator with a relative indication of audio phase correction.

4–138. **AUD, SEC, TER, DATA, VARI, AND SVO INDICATORS.** The record/playback unit front panel display circuit board contains the **AUD, SEC, TER, DATA, VARI,** and **SVO** indicators. The indicators provide status information on the various cartridge machine operating parameters. LOW control commands from the logic circuit board will be applied to illuminate the appropriate indicator as required. The following list presents the reference designator and description of each indicator.

INDICATOR	REFERENCE DESIGNATOR	DESCRIPTION
AUD	DS1	AUDIO INDICATOR
SEC	DS2	SECONDARY CUE TONE INDICATOR
TER	DS3	TERTIARY CUE TONE INDICATOR
DATA	DS4	DATA INDICATOR
VARI	DS5	VARI–SPEED MODE INDICATOR
SVO	DS6	SERVO MOTOR INDICATOR

4–139. **TAPE TIME/FUNCTION DISPLAY.** Tape time/function display DS12 is a four digit dot–matrix type display which provides PT–90 record/playback unit tape time and operating function information. The display is controlled by the microprocessor unit on CPU module. The microprocessor directs the operation of the display via: 1) address lines A0 through A2, 2) write line WR, and 3) data lines D0 through D7.

4–140. When the microprocessor is required to display tape time or operating function information, one digit of tape time/function display DS12 will be addressed via lines A0, A1, and A2. With the selected tape time/function display digit addressed, the WR line will go HIGH to initiate display write operations. Data from the CPU module will be routed through data lines D0 through D7 to display the appropriate information. The write cycle is repeated for the remaining tape time/function display digits.

4–141. **VU METER DISPLAY.** The VU meter display circuitry consists of green/red LED displays and the associated driver circuitry. The meter circuitry also contains peak detector circuits which generate control signals for application to the peak LED displays. The VU meter display contains identical left and right channel circuits; therefore, only the left channel will be described.

4–142. A varying dc control voltage input from the audio metering circuit on the record bias module is applied to integrated circuits U2 and U3. U2 and U3 are dot/bar display drivers which control the operation of the left channel meter display. The VU meter display consists of green 10–segment LED display DS8 and red 8–segment display DS9. U2 and U3 evaluate the applied input voltage and generate the appropriate control sequence to illuminate the segments of left channel meter display DS8 and DS9.

4–143. The peak audio circuitry consists of a driver circuit and two segments of LED display DS9. A varying dc control voltage from the peak detector circuit on the record bias module is applied to integrated circuits U6A and U6B. U6A and U6B are configured to function as a peak detector and hold circuit. When a dc input peak increases above a +2.8 volt comparator reference, the output of U6A will go HIGH. The HIGH is applied to: 1) U6B which outputs a LOW to illuminate the peak audio segments of LED display DS9 and 2) to charge an RC circuit consisting of resistor R9 and capacitor C4. The RC circuit maintains the comparator input voltage to allow the peak indicators to display momentary peak audio information. When the RC circuit discharges below the 2.8 volt reference, the output of U6B will go HIGH to extinguish the peak indicators.

4–144. **RECORD PREAMPLIFIER MODULE.**

4–145. **PROGRAM AUDIO CIRCUITRY.** Program record audio amplification, equalization, and input level monitoring is performed by circuitry on the record preamplifier module (refer to Figure 4–6). The program audio circuitry contains identical left and right channel circuits; therefore, only the left channel circuit will be discussed.

4–146. **Input Amplifier Circuit.** Left channel record input audio is applied to the audio circuitry through the module XLR connectors. A 600 Ohm input impedance is established by a resistive impedance network. Audio from the impedance network is applied to integrated circuits U1A, U1B, and U1D which are configured as an instrumentation amplifier. The amplifier is configured for a gain of one and designed to provide maximum input noise rejection.

4–147. Audio from the input amplifier is applied to an input level control stage consisting of integrated circuit U1C and potentiometer R10. U1C and R10 provide an input level control range from +20 dBm to –18 dBm.

4–148. **Input Indicator Circuit.** Samples from the input amplifier circuit are applied to an audio input indicator circuit consisting of a half–wave rectifier, a window comparator, and an indicator network. The samples are applied to integrated circuit U3B and diode D3 which are configured as a positive half–wave rectifier. The output from the half–wave rectifier is applied to window comparator U4C and U4D. When the voltage from the half–wave rectifier is between the upper and lower reference voltages, the outputs of U4C/U4D will go HIGH to bias driver transistor Q2 on and illuminate left channel input level indicator DS1. If the voltage increases above or decreases below the comparator reference voltages, the output of U4C/U4D will go LOW to bias Q2 off and extinguish indicator DS1.

4–149. **Record Audio/Test Tone Multiplexer Network.** Routing of record audio or test tone audio to the equalization and output buffer circuitry is controlled by multiplexer U5. When record audio processing is required, the CPU module will output a LOW through the test/normal control line to audio/test tone multiplexer U5. U5 will respond by routing record audio to the equalization/output buffer circuitry. When test tone audio processing is required, the test/normal control line will go HIGH to configure U5 to route test tone audio to the equalization/output buffer circuitry.

4–150. **Equalization, Level Control, and Output Buffer Networks.** Audio from audio/test tone multiplexer U5 is applied to integrated circuit U14A and potentiometer R47. U14A and R47 function as a low frequency equalization stage. The stage is designed to provide 6 dB of low frequency equalization.

4–151. The output of the low frequency equalization stage is applied to integrated circuit U6. U6 is a voltage–controlled–amplifier (VCA) module configured for precision control of the audio record level. The VCA is controlled by the CPU module. A varying dc voltage from the CPU is applied to the VCA which responds by increasing or decreasing the gain as required. The VCA is designed with a gain range of ±10 dB.

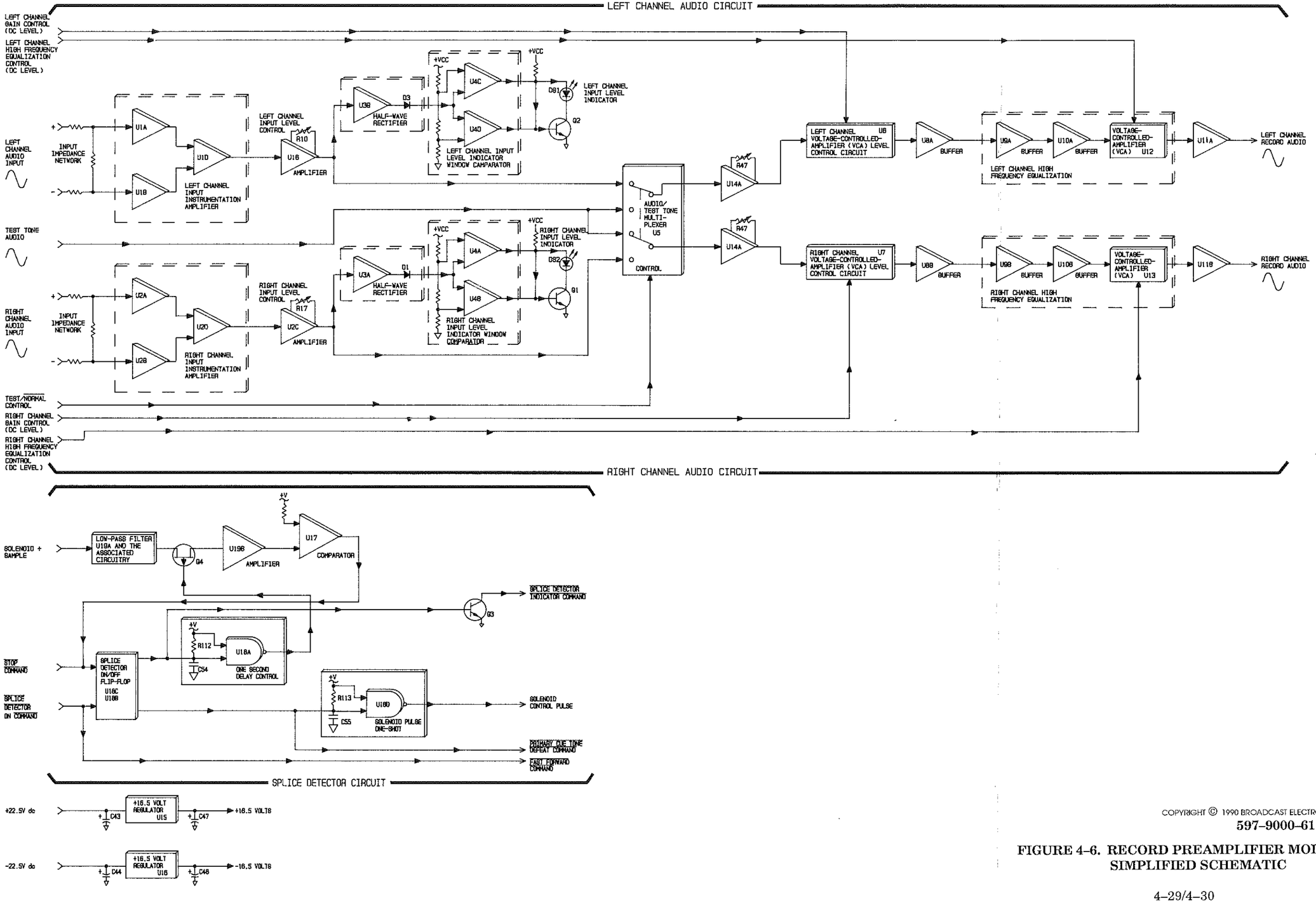


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FIGURE 4-6. RECORD PREAMPLIFIER MODULE SIMPLIFIED SCHEMATIC

4–152. Audio from the level control circuit is routed through buffer U8A to the left channel high frequency equalization network. The network consists of buffer stages U9A/U10A and voltage–controlled–amplifier (VCA) U12. The network is designed to provide ±5 dB of high frequency equalization.

4–153. The high frequency equalization network is controlled by the CPU module. A varying dc control voltage from the CPU is applied to the VCA which responds by increasing or decreasing the high frequency equalization as required.

4–154. Audio from the high frequency equalization network is applied to integrated circuit U11A. U11A buffers the output audio for application to the record bias module.

4–155. **Splice Detector Circuit.** All splice–find operations are directed by the splice detector circuit. The splice detector circuit automatically configures the unit to the fast–forward mode and stops at the cartridge tape splice for convenient record operations. The circuit locates tape splices by detecting a small solenoid voltage transient when the tape splice travels between the capstan shaft and the pressure roller.

4–156. The splice detector circuit responds to commands from the front–panel **SPL** switch/indicator. When the **SPL** switch/indicator is depressed, a LOW is applied to: 1) configure splice detector on/off control flip–flop constructed of NAND gates U18B/C to on and 2) enable the fast forward circuit on the logic module. Flip–flop U18B/C will respond by outputting HIGH and LOW control commands. A LOW command is routed to a solenoid control pulse circuit consisting of integrated circuit U18D, resistor R113, and capacitor C55. The circuit outputs a secondary solenoid drive pulse to ensure the solenoid is in the proper position for splice detection operations. A LOW is also routed to disable the primary cue tone detector.

4–157. A HIGH control command is applied to a one–second delay circuit consisting of integrated circuit U18A, resistor R112, and capacitor C54. After approximately one second as determined by resistor R112 and capacitor C54, U18A will output a LOW to enable transistor Q4 which controls the operation of a solenoid sample processing circuit.

4–158. The solenoid sample processing circuit consists of a low–pass filter, an amplifier stage, and a comparator. Solenoid voltage samples from the motherboard assembly are applied to a low–pass filter stage consisting of U19A and the associated circuitry. The output of the low–pass filter is applied through transistor Q4 to high–gain amplifier U19B. U19B is configured for a gain of approximately 200. The output of U19B is applied to comparator U17. When the solenoid voltage increases above the comparator reference, U17 will output a LOW to reset on/off flip–flop U18B/C and terminate splice find operations.

4–159. **Power Supply.** Operating potentials for record preamplifier module components are generated by a voltage regulator circuit. A +22.5 volt supply is processed into a +16.5 volt dc operating potential by regulator U15 and capacitor C47. A –22.5 volt supply is processed into a –16.5 volt dc operating potential by regulator U16 and capacitor C48.

4–160. RECORD BIAS MODULE.

4–161. Meter control operations, record bias processing, FSK encoding, and test tone generation are performed on the record bias module (refer to Figure 4–7). The record bias module is equipped with stereophonic program audio circuitry. The stereophonic circuitry contains identical left and right channel circuits; therefore, only the left channel circuit will be discussed.

4–162. **METERING CIRCUIT.** Control of the PT–90 record/playback unit multi–color VU meter display is provided by the record bias module metering circuitry. Meter switch commands, start indicator status, and record indicator status parameters are monitored by a control circuit consisting of inverters U19C/D and U21D/E/F and latch U18B. The circuit functions to direct the operation of meter audio multiplexer U30. U30 is designed to select audio samples such as left channel record, left channel playback, right channel record, right channel playback, cue channel playback audio, cue channel record audio, and record bias information for application to meter driver circuitry. Each audio sample is applied to multiplexer U30 through a potentiometer for meter calibration operations.

4–163. When the metering circuit is required to display playback audio information, a LOW from the start indicator control line is applied through inverters U19C and U21F and record meter programming jumper J702 to meter audio multiplexer U30. A LOW is also applied to U30 from latch U18B. Multiplexer U30 will respond by routing playback audio information to a meter rectifier circuit.

4–164. The metering circuit displays record audio information when the record indicator control line goes LOW. The LOW is inverted HIGH by U21D and applied to U30. With a LOW from latch U18B, multiplexer U30 will respond by routing record audio information to the meter rectifier circuit.

4–165. The display of record bias and cue channel audio information is controlled by the front panel **MTR** switch. When the **MTR** switch is depressed, a LOW is inverted HIGH by U19D and applied to latch U18B. U18B will output a HIGH to multiplexer U30 and to inverter U21E. U21E will output a LOW to illuminate the MTR switch/indicator. With a LOW applied from start indicator inverter network U19C and U21F, U30 will route cue channel playback information to the left channel meter circuit and record bias information to the right channel meter circuit. With a HIGH applied from inverter U21D, U30 will output cue channel record audio information to the left channel meter circuit and record bias information to the right channel meter circuit.

4–166. **Meter Rectifier Circuitry.** The meter rectifier circuitry consists of individual full–wave rectifier stages. Left channel meter audio is applied to amplifier stage U31D. U31D is configured for gain of approximately 8 dB. The output of U31D is applied to: 1) a peak full–wave rectifier circuit and 2) a left channel VU meter full–wave rectifier circuit.

4–167. Integrated circuit U31B and diodes D10 and D11 operate as a peak full–wave rectifier circuit. The rectified output is applied to the peak indicator circuitry on the front panel circuit board. Integrated circuit U31A and diodes D8 and D9 function as the left channel VU meter full–wave rectifier circuit. The rectified output of the circuit is applied through driver stage U31C for application to the left channel VU meter indicator circuitry.

4–168. **PROGRAM RECORD CIRCUIT.** Left channel record audio is routed to integrated circuit U1A which functions as an audio muting circuit. U1A is controlled by commands from the program bias control line. When record audio is required, the program bias on control line will go LOW. U1A will respond by routing audio through buffer stage U2A to left channel record head driver U3A.

4–169. **Record Bias Circuit.** A precision 128 kHz bias signal for application to the record heads is generated by the record bias circuit. A 2048 kHz reference signal from the CPU module is applied to bias frequency generator U8. U8 functions as a divider to output a 128 kHz bias signal to program bias control OR gate U9A. With the program bias on control line LOW, U9A will output the 128 kHz signal to bias level control circuit U6A. U6A is a CMOS multiplexer which processes a dc bias level signal from the CPU module and the 128 kHz signal to generate a precision square–wave bias signal at the appropriate amplitude.

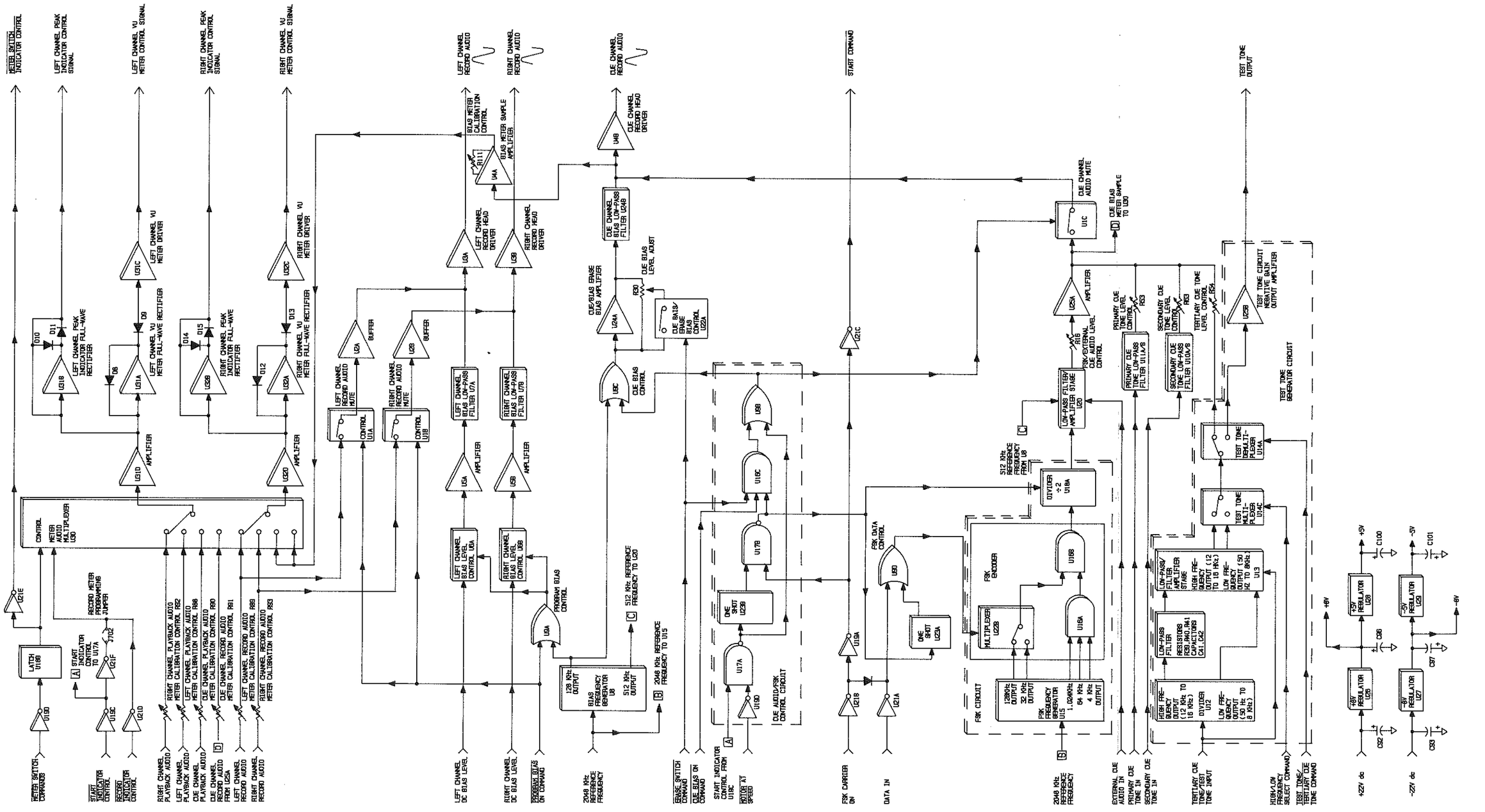

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FIGURE 4–7. RECORD BIAS MODULE SIMPLIFIED SCHEMATIC

4–170. The square–wave record bias signal from the bias level control circuit is applied to amplifier stage U5A. U5A is configured for a gain of approximately 2 dB. The output of U5A is applied to a low–pass filter stage consisting of U7A and the associated circuitry. The low–pass filter generates a sine–wave record bias signal for application to left channel record head driver U3A.

4–171. **CUE CHANNEL CIRCUIT.** The cue channel circuit consists of audio amplifier and control stages, bias circuitry, and cue tone processing networks. External cue channel record audio is applied to integrated circuit U20. U20 is a multi–function device which contains a low–pass filter stage and an amplifier stage. The external cue audio is routed through the amplifier stage of U20 to a second amplifier stage consisting of integrated circuit U25A. Potentiometer R16 provides external cue audio level control.

4–172. The output from amplifier U25A is applied to integrated circuit U1C which functions as an audio mute circuit. The operation of U1C is directed by a cue audio/FSK control circuit consisting of inverter U19D, NAND gates U17A/B, AND gate U16C, OR gate U9B, and one shot U23B. The circuit monitors cue bias, motor–at–speed, erase switch commands, start indicator, and FSK conditions to enable the appropriate circuitry. With a HIGH start indicator command, a LOW cue bias on command, and a LOW motor–at–speed command, U9B will output a LOW to U1C. U1C will respond by routing external cue audio to cue channel record head driver U4B.

4–173. **Cue Channel Bias Circuit.** The cue channel bias is produced by bias frequency generator U8. U8 outputs a precision 128 kHz square–wave signal to cue channel bias control gate U9C. With a HIGH start indicator command, a LOW cue bias on command, and a LOW motor–at–speed command, U9B will output a LOW to U9C. U9C will respond by routing the 128 kHz bias signal to amplifier stage U24A. U24A is a two–function amplifier designed to provide a low gain for cue bias operation and a high gain for cue channel erase operation. The gain of U24A is controlled by integrated circuit U22A and the front panel erase switch. With unit operated for cue bias operation, the erase switch control line will be HIGH. Integrated circuit U22A will respond by configuring cue bias level control potentiometer R30 into the feedback network of the amplifier stage to establish the appropriate gain for cue bias operations. The square–wave output of U24A is applied to a low–pass filter stage consisting of integrated circuit U24B and the associated circuitry. The low–pass filter generates a sine–wave bias signal for application to cue channel record head driver U4B.

4–174. **Primary Cue Tone Circuit.** The primary cue tone circuit consists of a low–pass filter network and a level control potentiometer. One kHz square–wave signals from the CPU module are applied to a two–section low–pass filter consisting of integrated circuits U11A/B and the associated circuitry. The low–pass filter provides square–wave to sine–wave signal conversion. The output of the filter is applied through potentiometer R53 to the cue channel audio mute circuit. Potentiometer R53 provides primary cue tone level control.

4–175. **Secondary Cue Tone Circuit.** The secondary cue tone circuit also consists of a low–pass filter network and a level control potentiometer. A 150 Hz square–wave signal from the CPU module is applied to a two–section low–pass filter consisting of integrated circuits U10A/B and the associated circuitry. The low–pass filter provides square–wave to sine–wave signal conversion. The output of the filter is applied through secondary cue tone level control potentiometer R63 for application to the cue channel audio mute circuit.

4–176. **Tertiary Cue Tone Circuit.** The tertiary cue tone is generated by a test tone generator circuit. The 8 kHz signal is applied through tertiary cue tone level control potentiometer R54 for application to the cue channel audio mute circuit. A detailed description of tertiary cue tone generation is presented in the test tone generator circuit discussion (refer to the following text).

4–177. **FSK ENCODER CIRCUIT.** All FSK information for application to the cue channel record head is processed by an FSK encoder circuit. The FSK circuit consists of a frequency generator, an encoder, a divider stage, and a low–pass filter section.

4–178. A 2048 kHz square–wave signal is applied to FSK frequency generator U5. U5 functions as a divider to generate 1.024 MHz, 64 kHz, 4 kHz, 128 kHz, and a 32 kHz frequencies for application to the FSK encoder circuit. The FSK encoder consists of multiplexer U22B and AND gates U16A/B. The encoder operates by shifting a carrier in response to the applied binary FSK information. Binary 1 information will generate a 7300 Hz output from the encoder. Binary 0 information will generate a 6700 Hz output from the encoder.

4–179. The output of the encoder is routed to integrated circuit U18A. U18A is configured as a divide–by–two stage to generate a 3650 Hz space frequency and a 3350 Hz mark frequency. The output of U18A is routed to integrated circuit U20. U20 is a two–function device which contains a low–pass filter stage and an amplifier stage. The FSK information is routed through the low–pass filter stage of U20 to generate a sine–wave output for application to FSK/external cue audio level control R16 and cue channel amplifier U25A.

4–180. The FSK encoder is controlled by a circuit consisting of inverters U21A/B and U19A, one shot U23A, and OR gate U9D. The FSK encoder may be enabled when: 1) the FSK carrier on line is HIGH and FSK data is applied to the circuit or 2) FSK data only is applied to the circuit. When the FSK carrier on line is HIGH, the HIGH is inverted by U21B and U19A for application to NAND gate U17B and inverter U21C. U17B and U21C generate a cartridge machine start command and initiate FSK encoder operation. When only FSK data is applied to the circuit, a HIGH FSK data signal will be inverted LOW by U21A. The LOW will be inverted HIGH by U19A to initiate cartridge machine and FSK encoder operation.

4–181. The HIGH from U19A is applied to U17B of the cue audio/FSK control circuit. With a HIGH start indicator control signal and a LOW motor–at–speed signal, U17B will NAND a HIGH from one shot U23B and the HIGH from inverter U19A. U17B will output a LOW to one shot U23A and to divider U18A. U23A delays the application of FSK data for approximately one second to prevent the recording of FSK information with a primary cue tone.

4–182. After the one second delay period, the output of U23A will go LOW. The LOW is applied to FSK control OR gate U9D. U9D will respond by routing the FSK data to the encoder circuit.

4–183. **TEST TONE GENERATOR CIRCUIT.** All PT–90 record/playback unit internal test tones are produced by a microprocessor controlled test tone generator circuit. The test tone generator circuit consists of a divider, low–pass filter/amplifier stage, a multiplexer network, and a output driver stage. The circuit generates all test tones for maintenance and alignment operations and also produces the tertiary cue tone signal.

4–184. **Test Tone Operation.** The test tone generator circuit is controlled by the microprocessor on the CPU module. The microprocessor controls the test tone circuit via the test tone/tertiary cue tone and high/low frequency select control lines. The circuit is configured for test tone operation when the microprocessor routes a HIGH to the circuit through the test tone/tertiary cue tone control line. The microprocessor will output a HIGH through the high/low frequency select line to configure the test tone generator circuit for the processing of a 12 kHz to 16 kHz test tone. A LOW control command will be routed through the frequency select line to configure the circuit for the processing of a 50 Hz to 8 kHz test tone.

4–185. When a test tone is required, the microprocessor will output a selected reference frequency through the tertiary cue tone/test tone input to divider U12. U12 is configured with a high frequency output port (12 kHz to 16 kHz) and a low frequency output port (50 Hz to 8 kHz). The high frequency output is routed to a passive low–pass filter consisting of resistors R39 through R41 and capacitors C41 and C42. The low frequency output is routed to the low–pass filter section of low–pass filter/amplifier stage U13. The low–pass filters stages provide square–wave to sine–wave signal conversion. The output of the passive low–pass filter is applied to the amplifier section of U13.

4–186. The high frequency (12 kHz to 16 kHz) and low frequency (50 Hz to 8 kHz) outputs from U13 are applied to a circuit consisting of multiplexer U14C and demultiplexer U14A. Multiplexer U14C and demultiplexer U14A are controlled by the microprocessor on the CPU module. The microprocessor will output a HIGH through the high/low frequency line to select a 12 kHz to 16 kHz test tone. A LOW will be output through the high/low frequency control line to select a 50 Hz to 8 kHz test tone.

4–187. The output of multiplexer U14C is applied to demultiplexer U14A. U14A is designed to route a tertiary cue tone signal or a test tone signal to the appropriate circuit. With the circuit configured for test tone operation, the microprocessor will output a HIGH to U14A. U14A will respond by routing the test tone signal through negative gain output amplifier U25B to the preamplifier module.

4–188. **Tertiary Cue Tone Operation.** The test tone generator circuit also produces the tertiary cue tone. When tertiary cue tone operation is required, the microprocessor will output a reference frequency through tertiary cue tone/test tone input to divider U12. U12 will output an 8 kHz signal through the low frequency output to the low–pass filter section of U13 for square–wave to sine–wave signal conversion. The output of U13 is routed to multiplexer U14C.

4–189. To configure multiplexer/demultiplexer circuitry for tertiary cue tone operation, the microprocessor will output a LOW to multiplexer U14C and a LOW to demultiplexer U14A. U14C and U14A will respond by routing the signal through tertiary cue tone level adjust control R54 for application to the cue channel circuitry.

4–190. **POWER SUPPLY CIRCUIT.** The record bias module power supply circuit consists of positive and negative regulator and filter networks. A +22 volt potential from the power supply module is regulated into a +10 volt dc supply by regulator U26 and capacitor C96. The +10 volt supply is re–regulated into a +5 volt supply by regulator U28 and capacitor C100.

4–191. A –22 volt supply from the power supply module is regulated into a –10 volt dc potential by regulator U27 and capacitor C97. The –10 volt supply is re–regulated into a –5 volt dc potential by regulator U29 and capacitor C101.

4–192. **CPU MODULE.**

4–193. **GENERAL.** All PT–90 record/playback unit record operations are controlled by the CPU module (refer to Figure 4–8). The CPU module contains an Intel 80C39 microprocessor which monitors and executes the record operating functions. Input/output interface circuitry is incorporated into the design to expand the monitoring and control capabilities of the microprocessor. The microprocessor memory circuit consists of: 1) a read–only–memory (ROM) integrated circuit which contains the microprocessor control program and 2) a non–volatile random–access–memory (RAM) integrated circuit for the storage of tape cartridge operating parameters.

4–194. **READ–ONLY–MEMORY (ROM).** The microprocessor read–only–memory (ROM) consists of integrated circuit U7. U7 is a 8192 byte EPROM which provides a permanent location for the PT–90 record/playback unit microprocessor instruction code. The code directs the operation of all microprocessor control functions.

4–195. **RANDOM–ACCESS–MEMORY (RAM).** The microprocessor random–access–memory (RAM) is implemented on integrated circuit U8. U8 is a 2K x 8 non–volatile RAM device. The device provides a stable environment for the storage of audio tape operating characteristics and prevents the loss of data when power is removed.

4–196. **MICROPROCESSOR.** Integrated circuit U3 is an Intel 80C39 microprocessor which is configured to monitor and execute all record operations. U3 contains an 8–bit bidirectional data bus and two 8–bit bidirectional communication ports. The data bus provides internal address and data communication to the memory circuit and a signal generating circuit. The communication ports are used for both address and data communication to external devices.

4–197. The 80C39 microprocessor is equipped with control signals for communication to associated digital circuitry. The commands are used to synchronize microprocessor operations. The following list presents a description of the microprocessor control signals.

MICROPROCESSOR COMMAND	DESCRIPTION
READ (RD)	A LOW–active processor command to read information from memory.
WRITE (WR)	A LOW–active processor command to write information to memory or the signal generator circuit.
PROGRAM STORE ENABLE (PSEN)	A LOW–active processor command to enable ROM circuit and access instructions.
ADDRESS LATCH ENABLE (ALE)	A HIGH–active processor command to enable the memory circuit address latch.
PROTOCOL (PROG)	A HIGH–active processor command to enable the interface circuitry.

4–198. **MICROPROCESSOR CRYSTAL OSCILLATOR.** Microprocessor U3 operates from a precision 6.144 MHz reference signal. The reference is generated by crystal oscillator Y1 and capacitors C5 and C6.

4–199. **INTERRUPT SIGNAL GENERATOR.** An interrupt is a synchronization command which temporarily suspends microprocessor operation. The interrupt signal generator consists of latch U11A. U11A is controlled by a 1 Hz tachometer pulse from the motor control circuit board. U11A will output LOW interrupt commands to the microprocessor at a 1 Hz rate. The microprocessor responds to an interrupt command by routing a HIGH interrupt acknowledge command to set latch U11A. The interrupt commands are also used by the microprocessor for the display of tape time information.

4–200. **ADDRESS CIRCUITRY.** The microprocessor addressing operations utilize: 1) the 8–bit bidirectional address/data bus, 2) the port 2 4–bit bidirectional address/data bus, and 3) address latch U6. The circuitry provides communication between the microprocessor and the ROM, RAM, and input/output expander circuitry.

4–201. **ROM Addressing Operations.** When microprocessor U3 is required to read information from EPROM U7, U3 will generate a 12–bit address. 8 bits of the address are applied to the 8–bit bidirectional address/data bus. The remaining 4 bits of the address are applied through the port 2 bidirectional address/data bus.

4–202. During the EPROM read cycle, the microprocessor will output the 12–bit address for application to U7. The PSEN line will go LOW to enable EPROM U7 and the ALE line will go HIGH to enable address latch U6. 4 address bits are routed directly to U7. 8 address bits are routed to address latch U6. U6 stores the address bits to release the address/data bus for data communication. Once the address data is stored, the ALE line will go LOW. The LOW instructs U6 to route the remaining 8 address bits to U7. With a memory location addressed, information will be read from the location and routed to the microprocessor via the 8–bit address/data bus.

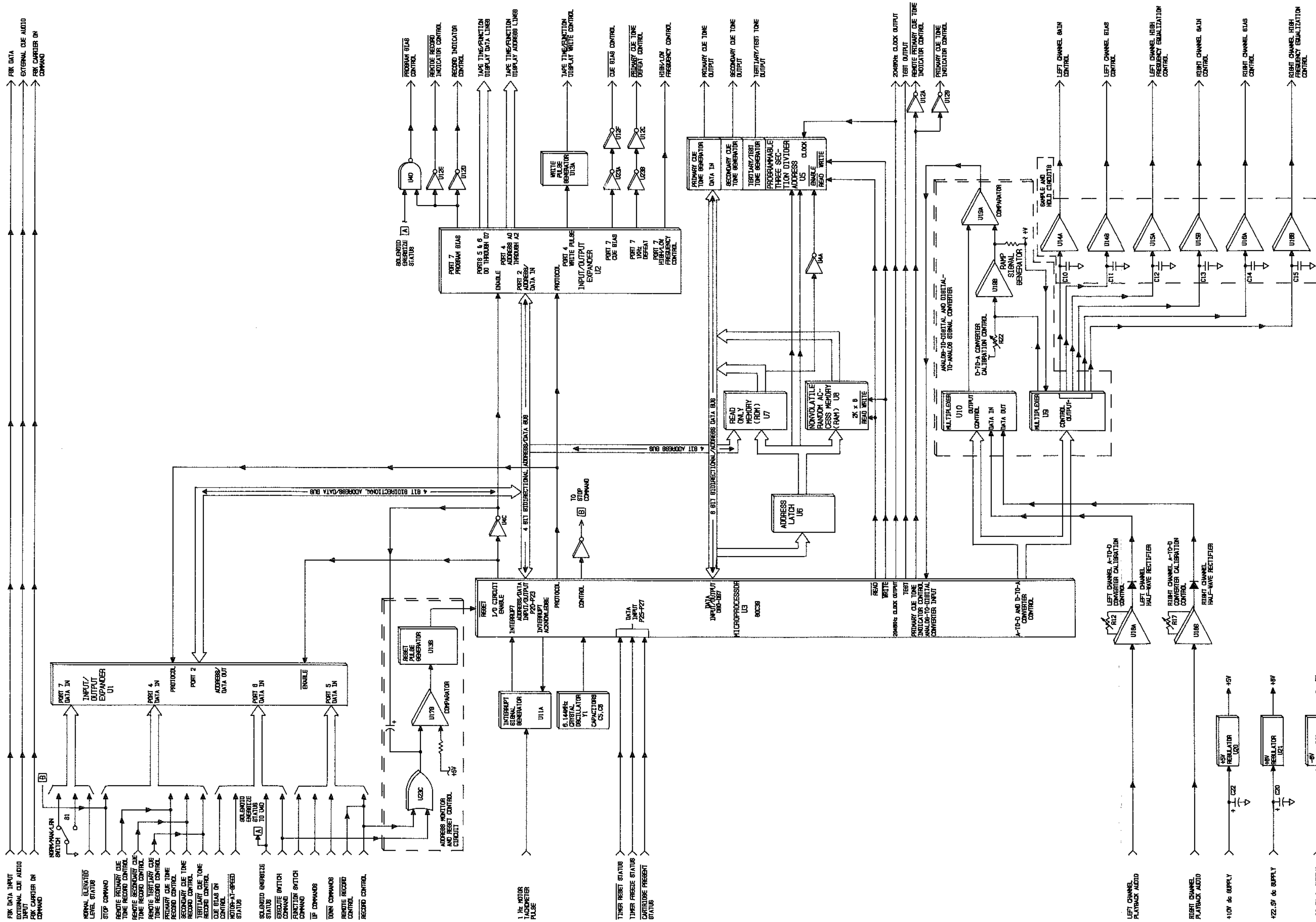

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FIGURE 4-8.
CPU MODULE SIMPLIFIED SCHEMATIC

4–203. **RAM Addressing Operations.** When the microprocessor is required to read or write information to RAM, a RAM address cycle is initiated to select a memory location. The microprocessor ALE line will go HIGH to enable latch U6. An 8 bit address from U3 will be routed through the bidirectional data bus and stored in latch U6. The ALE will go LOW which configures U6 to route the address to RAM integrated circuit U8. With a memory location addressed, data will be: 1) written into the location if the WR line is LOW or 2) read from the location if the RD line is LOW.

4–204. **MICROPROCESSOR INPUT/OUTPUT INTERFACE CIRCUITRY.** Due to the monitoring and control requirements of the PT–90 record/playback design, the microprocessor is designed with input/output expansion circuitry. Integrated circuits U1 and U2 are input/output expansion devices designed to increase the interfacing capabilities of the microprocessor. Expansion device U1 is configured to monitor record functions and internal status conditions. Expansion device U2 is configured to communicate with the front–panel tape time/function display, internal control signals, and the test tone generator circuit. The following list presents input/output expander signal communication.

INPUT/OUTPUT EXPANDER U1 COMMUNICATION

1. Cue bias on switch.
2. Record switch.
3. Function switch.
4. Up switch.
5. Down switch.
6. Motor–at–speed status.
7. Solenoid status.
8. Execute switch.
9. Normal/elevated level status.
10. Manual/normal/learn switch.
11. Primary cue tone record switch.
12. Secondary cue tone record switch.
13. Tertiary cue tone record switch.

INPUT/OUTPUT EXPANDER U2 COMMUNICATION

1. Tape time/function display.
2. Cue bias on control.
3. Primary cue tone defeat control.
4. Test tone generator circuit.
5. Program bias control.

4–205. **Input/Output Expander U1 Operation.** When the microprocessor is required to read record functions or status information from input/output expander U1, the protocol line will go HIGH and the input/output expander enable line will go LOW. A 4–bit input/output expander port identification address will be routed through the port 2 bidirectional address/data bus to U1. U1 will decode the address and route the requested information to the microprocessor through the address/data bus.

4–206. **Input/Output Expander U2 Operation.** When microprocessor U3 is required to: 1) display information on the tape time/function display, 2) enable the cue bias, 3) disable the primary cue tone circuit, or 4) control the test tone generator circuit, the microprocessor will address and write data to input/output expander U2. The microprocessor protocol line and the input/output expander enable line will go HIGH. A 4–bit input/output expander port identification address will be routed through the port 2 address/data bus to U2. U2 will decode the address and enable the selected data port.

4–207. When display of tape time or record function information is required, the microprocessor will initiate a tape time/function display address and write cycle. Microprocessor U3 will address and route a 3–bit tape time/function display address and a 1–bit write command to port 4 of input/output expander U2. U2 will: 1) output the address to the tape time/function display and 2) output a LOW command to trigger write pulse generator U13A. U13A will route a LOW write command to the tape time/function display. The cycle is completed when U3 addresses and routes two 4–bit data words through the address/data bus to ports 5 and 6 of U2 for application to the tape time/function display.

4–208. Microprocessor U3 controls program and cue bias, primary cue tone defeat operation, and test tone frequency selection from port 7 of U2. When a program bias on command is required, U3 will address and output a 4–bit code to port 7 of U2. U2 will output a HIGH to inverters U12D/E and to AND gate U14D. U14D ANDs the HIGH from U2 and a HIGH solenoid status to generate a LOW program bias enable command. The output of inverters U12D/E will go LOW to illuminate the record indicators. Cue bias on commands from microprocessor U3 are also applied to port 7 of U2. U2 will output a LOW through inverters U23A and U12F to produce a LOW cue bias on command.

4–209. Primary cue tone defeat and test tone frequency selection commands are also processed through port 7 of U2. When the microprocessor is required to defeat the primary cue tone detection circuitry, U3 will address and output a 4–bit code to U2. U2 will output a LOW through inverters U23B and U12C to disable the primary cue tone detection circuit. U3 will also output a 4–bit code to U2 for test tone frequency selection commands. When a high frequency test tone (12 kHz to 16 kHz) is required, U3 will route the appropriate code to U2. U2 will output a HIGH to configure the test tone generator circuit for a high frequency test tone. A LOW will be routed to the test tone generator circuit to select a low frequency test tone (50 Hz to 8 kHz).

4–210. **ADDRESS MONITOR AND RESET CONTROL CIRCUIT.** Microprocessor reset commands are generated by a circuit consisting of OR gate U23C, comparator U17B, one–shot U13B. A reset command is generated when the **EXEC** and **REC** switches are simultaneously depressed. LOW control commands from the switches are gated at U23C. OR gate U23C outputs a LOW to comparator U17B. With the control input below the comparator reference, the output of U17B will go HIGH and trigger reset pulse generator U13B. The output of U13B will go LOW to reset the microprocessor.

4–211. The control circuit also monitors microprocessor addressing activity and generates an automatic reset signal during an operating failure. During a microprocessor failure, the absence of constant addressing activity will produce a LOW from inverter U4C. The LOW is applied to comparator U17B. The output of U17B will go HIGH to generate a LOW reset command from reset pulse generator U13B.

4–212. **TEST/CUE TONE GENERATION.** All PT–90 record/playback unit cue and test tones are generated by microprocessor U3 and divider U5. U5 is a programmable three–section divider which is configured to generate: 1) primary, secondary, and tertiary cue tones and 2) eight test tone frequencies (50 Hz, 125 Hz, 500 Hz, 1 kHz, 4 kHz, 8 kHz, 12 kHz, and 16 kHz).

4–213. Microprocessor U3 will initiate a cue/test tone divider U5 addressing cycle when cue or test tones are required. U3 will output a 2–bit address through the address/data bus to U6. The ALE line will go HIGH which instructs latch U6 to store the applied information. Once the data is stored, the ALE line will go LOW. The LOW instructs latch U6 to route the address to divider U5.

4–214. After the application of the divider address information, microprocessor U3 will route an 8–bit data code through the address/data bus to program divider U5. U5 consists of a primary cue tone section, a secondary cue tone section, and a tertiary/test tone section. When programmed to generate a primary or secondary cue tone, U5 will: 1) output a 128 kHz square–wave signal from the primary cue tone section or 2) output a 19.2 kHz square–wave signal from the secondary cue tone section.

4–215. When divider U5 is programmed for tertiary cue tone or test tone operation, the divider requires the operation of two additional control lines for tone generation. The microprocessor TEST control line and the high/low frequency control line from port 7 of U2 are required to route the selected signal through the test tone generator circuit on the record bias module. A tertiary cue tone is generated when microprocessor U3 outputs the appropriate data to divider U5. The tertiary/test tone section will respond by generating a 102.4 kHz signal for application to the test tone generator circuit on the record bias module. The microprocessor TEST control line will go LOW and the high/low frequency control line from input/output expander U2 will go LOW. The control signals configure the test tone generator circuit on the record bias module to output an 8 kHz tertiary cue tone signal.

4–216. Test tones are also generated by the tertiary/test tone section of U5 and the microprocessor control signals. When a low frequency test tone (50 Hz to 8 kHz) is required, microprocessor U3 will address and output the appropriate data to divider U5. The tertiary test tone section will respond by generating a signal at 128 times the tone frequency for application to the test tone generator circuit on the record bias module. The microprocessor TEST control line will go HIGH and the high/low frequency control line from input/output expander U2 will go LOW. The control signals configure the test tone generator circuit on the record bias module to output the selected frequency to the record audio circuitry. When a high frequency test tone (12 kHz to 16 kHz) is required, the tertiary/test tone section will respond by generating a signal at 2 times the tone frequency. The TEST control line will go HIGH and the high/low frequency control line will go HIGH to configure the test tone circuit on the record bias module to output the selected frequency.

4–217. **ANALOG–TO–DIGITAL (A–TO–D) CONVERTER CIRCUIT.** The microprocessor monitors and evaluates audio parameters such as record level, record bias, and high frequency equalization from information generated by an analog–to–digital (A–to–D) converter circuit. The A–to–D converter circuit consists of multiplexers U9 and U10, ramp signal generator U19B, comparator U19A, and left and right channel half–wave rectifier sample circuits.

4–218. Audio samples for application to the A–to–D converter are generated by left channel half–wave rectifier U18A and right channel half–wave rectifier U18B. Left channel potentiometer R12 and right channel potentiometer R17 provide A–to–D converter calibration. An A–to–D converter sampling cycle is initiated when microprocessor U3 is required to establish record level, record bias, or high frequency equalization parameters. U3 will addresses multiplexer U9. U9 will respond by shorting the output of U19B to the input. As a result, the ramp signal generator will be reset.

4–219. With the ramp signal generator reset, microprocessor U3 will address multiplexer U10. U10 will respond by routing either the left or right channel sample to comparator U19A. U19B will respond by routing a ramp generator signal to comparator U19A. When the voltage from the ramp generator is equal to the sample voltage, the output of comparator U19A will go LOW. The LOW is routed to microprocessor U3 which measures the amount of time between initial ramp generator operation and the change in the output state of comparator U19A. U3 evaluates the sampled time for the selected operating parameter (record level, record bias, or high frequency equalization) and determines if an increase or decrease is required.

4–220. **DIGITAL–TO–ANALOG (D–TO–A) CONVERTER CIRCUIT.** Multiplexers U9 and U10, ramp generator U19B, and comparator U19A also function as a digital–to–analog (D–to–A) signal converter. The circuit processes digital commands and outputs dc levels through individual sample and hold circuits for control of record level, record bias, and high frequency equalization.

4–221. A D–to–A converter cycle is initiated when microprocessor U3 addresses multiplexer U9. U9 will reset the ramp signal generator by shorting the output of U19B to the input. With all reset operations completed, ramp signal generator U19B will begin operation. Microprocessor U3 will begin a waiting sequence which is equal to the output voltage to be established. After completion of the selected waiting period, U3 will address multiplexer U9. U9 will respond by routing the accumulated ramp voltage to a sample–and–hold circuit. Potentiometer R22 provides calibration of the D–to–A signal converter.

4–222. Integrated circuits U14A/B, U15A/B, and U16A/B and the associated capacitors are configured as sample and hold circuits. The sample and hold circuits process the ramp generator voltages from U19B into a stable dc voltage for application to the record level, record bias, or high frequency equalization control circuits on the preamplifier and record bias modules.

4–223. **POWER SUPPLY CIRCUIT.** The CPU module power supply circuit consists of positive and negative regulator and filter networks. A +10 volt dc supply from the power supply module is regulated into a +5 volt supply by regulator U20. Capacitor C22 provides input filtering. A +22 volt dc supply is processed into a +8 volt potential by capacitor C20 and regulator U21. A –22 volt supply is regulated into a –8 volt potential by regulator U22 and capacitor C21.

SECTION V
MAINTENANCE

5–1. INTRODUCTION.

5–2. This section provides general maintenance information, mechanical and electrical adjustment procedures, and troubleshooting information for the Broadcast Electronics PT–90 series cartridge machines.

5–3. SAFETY CONSIDERATIONS.

5–4. Low voltages are used throughout PT–90 series cartridge machine audio, logic, display, and control modules. Maintenance with power energized is always considered hazardous and caution should be observed. Good judgment, care, and common sense must be practiced to prevent accidents. The procedures contained in this section should be performed only by experienced and trained maintenance personnel.

5–5. FIRST LEVEL MAINTENANCE.

5–6. First level maintenance consists of precautionary procedures applied to the equipment to prevent future failures. The procedures are performed on a regular basis and the results recorded in a maintenance log.

WARNING *DISCONNECT ALL CARTRIDGE MACHINE PRIMARY POWER BEFORE ATTEMPTING ANY EQUIPMENT MAINTENANCE.* *WARNING*

5–7. GENERAL.

5–8. Periodically remove abrasions from the cartridge machine chassis with a cloth moistened with a mild household cleaner. Remove dust from the chassis exterior with a brush and vacuum cleaner as required.

5–9. ELECTRICAL.

5–10. The cartridge machine circuitry should be periodically cleaned of accumulated dust using a brush and vacuum cleaner. Check the circuit boards for improperly seated semiconductors and components damaged by overheating.

5–11. MECHANICAL.

WARNING *MOST SOLVENTS WHICH REMOVE TAPE RESIDUE ARE VOLATILE AND TOXIC BY NATURE AND MUST BE APPLIED IN SMALL AMOUNTS IN A WELL VENTILATED AREA. OBSERVE THE SOLVENT CONTAINER SAFETY INFORMATION AND DO NOT USE THE SOLVENT NEAR FLAME, CIGARETTES, AND HOT SOLDERING IRONS.* *WARNING*

WARNING

5–12. Each day clean the heads, tape guides, pressure roller, and capstan shaft with a cleaning solvent to remove accumulated oxide. Recommended cleaning solvents include: 1) Broadcast Electronics head cleaning kit 979–0064 and 2) isopropyl alcohol. The pressure roller and capstan shaft may be cleaned utilizing the cartridge machine maintenance mode operation (refer to MAINTENANCE MODE OPERATION in SECTION III, OPERATION).

5–13. Approximately once a week, demagnetize the heads and other ferrous components in the tape path. Perform the demagnetizing with an appropriate degausser. Observe the degausser operating instructions to prevent damage to the heads.

5–14. **TAPE CARTRIDGES.**

5–15. **TAPE CARTRIDGE DIAGNOSTICS.** The PT–90 record/playback unit is equipped with a tape cartridge diagnostic feature. When operated in the LEARN mode, the unit will diagnose a defective tape cartridge and display FAIL in the tape/time function display if a cartridge exceeds preset record compensation levels. To operate the record/playback unit in the LEARN mode, refer to procedures described in SECTION III, OPERATION.

5–16. **SCOTCHCART ® ADJUSTMENT TOOL.** Each PT–90 cartridge machine is equipped with an adjustment tool (BE P/N 800–5001) for the alignment of SCOTCHCART ® tape cartridges (located in the Accessory Parts Kit). Refer to the SCOTCHCART ® tape cartridge service information for alignment and maintenance procedures.

5–17. SECOND LEVEL MAINTENANCE.

5–18. Second level maintenance consists of procedures required to restore a PT–90 series cartridge machine to operation after a fault has occurred. The procedures are divided into mechanical adjustments, electrical adjustments, mechanical component replacement procedures, electrical component replacement procedures, and troubleshooting.

5–19. The PT–90 series cartridge machine maintenance philosophy consists of isolating a problem to a specific assembly with subsequent troubleshooting to isolate defective components. The defective components may be repaired locally or the entire assembly may be returned to Broadcast Electronics, Inc. for repair or replacement.

5–20. **MECHANICAL ADJUSTMENTS.**

5–21. The following text provides adjustment procedures for mechanical components associated with the PT–90 series cartridge machines. The procedures are presented in the following order.

ADJUSTMENT PROCEDURES

A. Motor Alignment Procedure.

B. Pinch Roller Indentation Adjustment.

C. Solenoid Response Adjustment.

D. Head Adjustments.

5–22. The following test equipment is required for the mechanical adjustment procedures. Refer to the following list as required for each procedure.

TEST EQUIPMENT

A. Calibrated Oscilloscope, 5 MHz Bandwidth, Dual Channel With Lissajous Display of Inputs.

B. Tape Head and Tape Guide Alignment Gauge (BE P/N 300–0002).

C. Motor Alignment Gauge (BE P/N 300–0700).

D. Pressure Roller Indentation Gauge (BE P/N 300–0013).

E. Allen Wrenches (supplied with the Cartridge Machine).

SCOTCHCART ® is a registered trademark of 3M.

F. Tape Alignment Cut–Away Test Cartridge (BE P/N 710–0132).

G. Stereophonic Reproduce Alignment Tape (BE P/N 800–1005). Monophonic Reproduce Alignment Tape (BE P/N 800–1005–001).

H. No. 1 Phillips Screwdriver, 4 Inch (10.2 cm) Blade.

5–23. **MOTOR ALIGNMENT PROCEDURE.** The deck pressure roller operates in conjunction with the motor capstan shaft to provide tape movement. The pressure roller and the motor capstan shaft must be properly aligned to prevent improper tape movement across the heads.

5–24. **Procedure.** To align the cartridge machine motor and deck solenoid, proceed as follows:

5–25. Disconnect the cartridge machine primary power.

5–26. Manually retract the deck solenoid plunger (refer to Figure 5–1) and remove the pressure roller E–ring, pressure roller, and the nylon washers.

5–27. Refer to Figure 5–2 and loosen the two motor mounting screws to allow movement of the motor assembly.

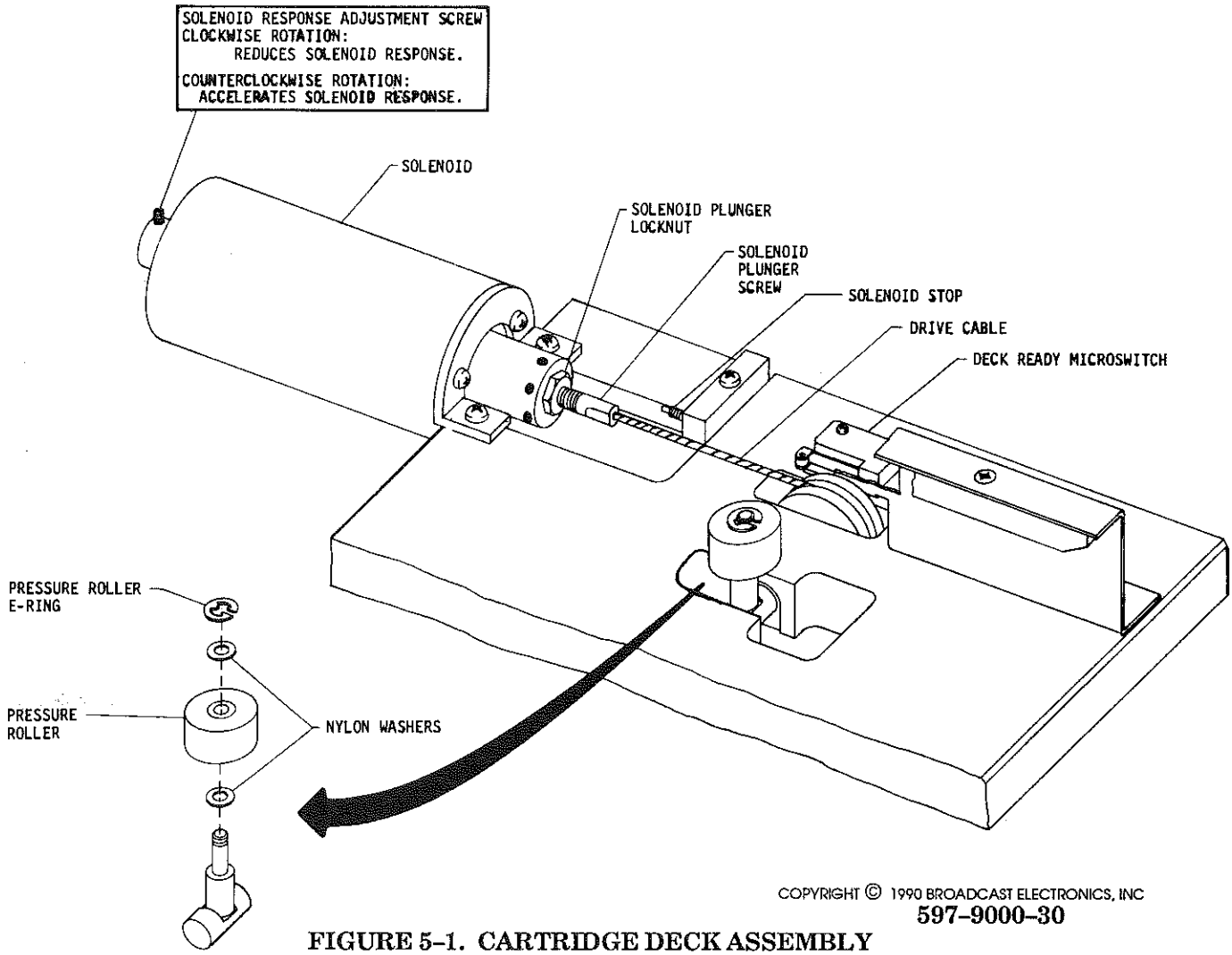

FIGURE 5–1. CARTRIDGE DECK ASSEMBLY

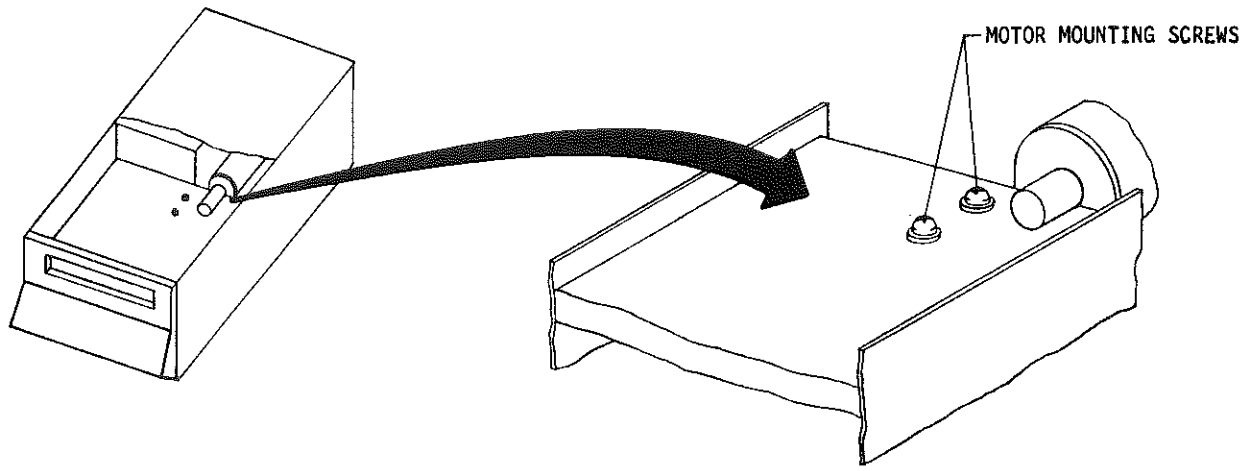

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FIGURE 5-2. MOTOR MOUNTING SCREWS

5–28. Refer to Figure 5–3A and place motor alignment gauge 300–0700 on the deck pressure roller shaft.

5–29. Refer to Figure 5–3A and move the motor assembly until the capstan shaft is tangent with the alignment gauge.

5–30. Secure the two motor mounting screws. Secure the screws alternately to ensure correct motor alignment. Remove the alignment gauge.

5–31. Refer to Figure 5–1 and re–install the pressure roller, the nylon washers, and the pressure roller E–ring.

5–32. **PRESSURE ROLLER INDENTATION ADJUSTMENT.** This procedure adjusts the correct pressure roller indentation. Proper pressure roller indentation determines the amount of tape pull. Refer to Figure 5–3 and coarse adjust the solenoid plunger as follows:

A. Disconnect the cartridge machine primary power.

B. Loosen the solenoid plunger locknut.

C. Rotate the solenoid plunger clockwise or counterclockwise as required until the plunger front–surface is aligned with the solenoid bracket.

D. Finger tighten the solenoid plunger locknut.

CAUTION ***WHEN OPERATING THE DECK SWITCH TO THE ON POSITION, DO NOT USE A METALLIC OBJECT.***

CAUTION

5–33. Fine adjustment of the pressure roller indentation begins by allowing the solenoid to cool for 2 hours. Once the solenoid is cool, temporarily operate the deck switch to the ON position.

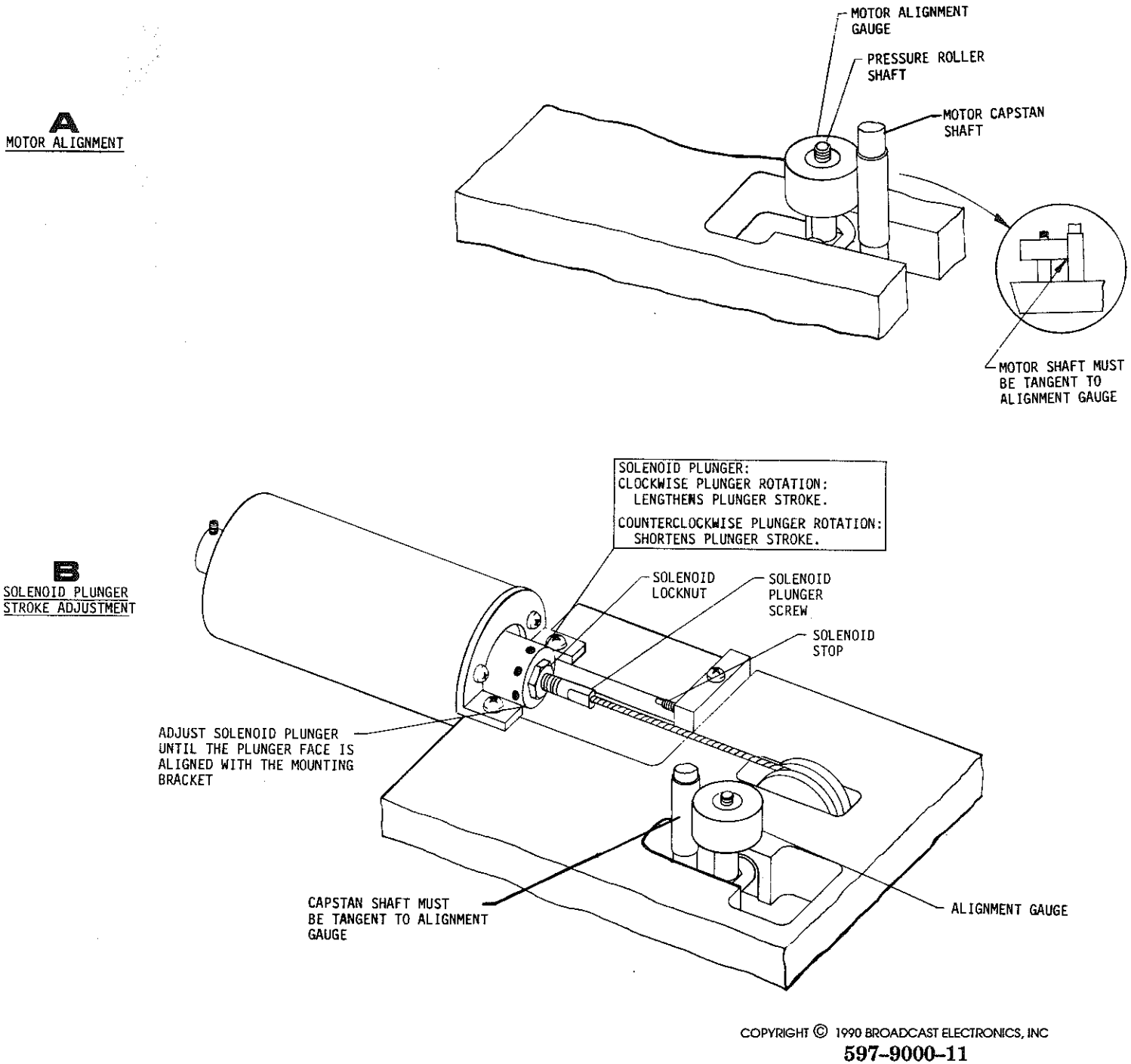

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FIGURE 5-3. MOTOR ALIGNMENT

5–34. Apply power to the cartridge machine. Depress the deck start switch/indicator to energize the solenoid.

WARNING ***MAINTENANCE WITH MOVING PARTS IS ALWAYS CONSIDERED HAZARDOUS AND CAUTION SHOULD***

WARNING ***BE OBSERVED. DO NOT TOUCH THE CAPSTAN SHAFT OR THE PRESSURE ROLLER SHAFT WITH THE PARTS IN MOTION.***

5–35. Fine adjustment of the pressure roller indentation is accomplished by using the pressure roller indentation gauge as shown in Figure 5–4. Insert the gauge between the capstan shaft and pressure roller shaft in the direction indicated while maintaining the gauge perpendicular to the deck surface.

5–36. Refer to Figure 5–4 and adjust the pressure roller indentation by rotating the solenoid plunger clockwise to decrease distance D or counterclockwise to increase distance D as required. Correct adjustment is obtained when the gauge will pass between the shafts with a slight resistance. Deenergize the solenoid between measurements to allow the solenoid to stabilize.

5–37. Once the correct pressure roller indentation is obtained, refer to Figure 5–1 and adjust the solenoid plunger stop until the pressure roller is just below the deck surface when the solenoid is deenergized.

5–38. Disconnect the cartridge machine primary power. Secure the solenoid plunger locknut and restore the deck switch to normal operation.

5–39. **SOLENOID RESPONSE ADJUSTMENT.** The solenoid is equipped with a control to adjust the response of the plunger. The control adjusts the rate of air movement through a relief valve to establish the response of the plunger and the level of noise generated. The control is factory adjusted for a compromise between response and noise level. Generally, the solenoid response will not require adjustment. However, the response may be adjusted to obtain any individual requirements. The solenoid response is adjusted as follows.

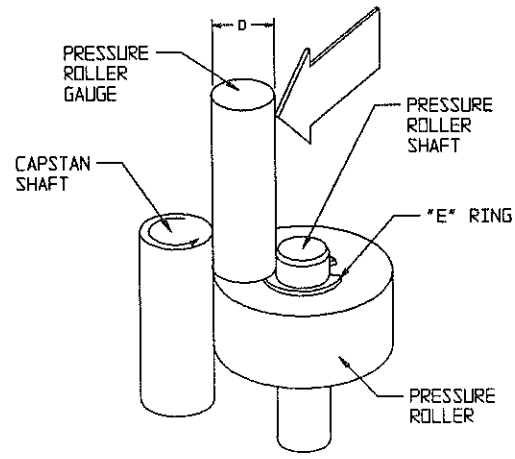

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FIGURE 5–4. PRESSURE ROLLER INDENTATION ADJUSTMENT

5–40. **Procedure.** To adjust the solenoid response, proceed as follows:

5–41. Disconnect the cartridge machine primary power.

5–42. Refer to Figure 5–9C and adjust solenoid response control **AIR DAMP ADJ** clockwise 1/4 of a revolution to reduce the response and decrease the noise level of the solenoid. Adjust the solenoid response control counterclockwise 1/4 of a revolution to accelerate the response and increase the noise level of the solenoid.

5–43. Perform an operational test to ensure the deck performs as desired. If required, repeat the procedure to obtain the desired results.

CAUTION

CAUTION

TO PREVENT DAMAGE TO THE PHASE LOK V HEAD ASSEMBLY, PERFORM ALL HEAD ASSEMBLY ADJUSTMENTS USING THE ALLEN WRENCH PROVIDED WITH THE UNIT.

5–44. **HEAD ADJUSTMENTS.** The head adjustments involve the alignment of the tape guide height, head height, head zenith, head azimuth, and head phase response parameters. The head parameters are presented as individual adjustment procedures. Due to the design of the PHASE LOK V head bracket, only head azimuth and the related electrical parameters will require periodic adjustment (example: prior to extensive continuous operation). The following list presents the procedures required for periodic maintenance. When a replacement head is installed, all head adjustment procedures must be performed (refer to the HEAD REPLACEMENT PROCEDURE specific replacement information).

PERIODIC PLAYBACK HEAD ADJUSTMENT PROCEDURES

MONOPHONIC CARTRIDGE MACHINES

A. The Playback Head Azimuth Adjustment Procedure.

B. The PLAYBACK EQUALIZATION Procedure.

STEREOPHONIC CARTRIDGE MACHINES

A. The Playback Head Azimuth Procedure.

B. The Playback Phase Response Adjustment Procedure.

C. The PLAYBACK EQUALIZATION Procedure.

PERIODIC RECORD HEAD ADJUSTMENT PROCEDURES

STEREOPHONIC CARTRIDGE MACHINES

A. The Record Head Azimuth Adjustment Procedure.

B. The Record Head Phase Response Adjustment Procedure.

5–45. The following text presents adjustment procedures for the playback, dummy, and record heads. For playback only models, align the playback head before adjusting the dummy head. For record/playback models, align the playback head before adjusting the record head.

5–46. An adjustment tool (located in the Accessory Parts Kit) is provided with the unit for head assembly alignment. Perform all head alignment procedures using the adjustment tool.

5–47. **Tape Guide Height Adjustment Procedure.** To ensure proper tape movement, perform the tape guide height adjustment procedure for each tape guide. To adjust the tape guide height, proceed as follows:

5–48. Refer to Figure 5–5A and check the tape guide height. The inside edge of the upper tape guide must be aligned with the top surface of the alignment gauge.

5–49. If adjustment is required, refer to Figure 5–6 and loosen the tape guide adjustment screws.

5–50. Adjust the tape guide to obtain proper alignment.

5–51. Secure the tape guide adjustment screws.

5–52. **Head Height Adjustment Procedure.** To adjust the playback, record, or dummy head height, proceed as follows:

5–53. Refer to Figure 5–5B and check the playback or record head height. The head upper pole must be aligned with the top of the alignment gauge.

5–54. Insert the tape alignment cut–away test cartridge into the cartridge deck and begin deck operation to visually inspect the tape movement across the heads. The magnetic tape must cover the top and bottom of the head poles (refer to Figure 5–7).

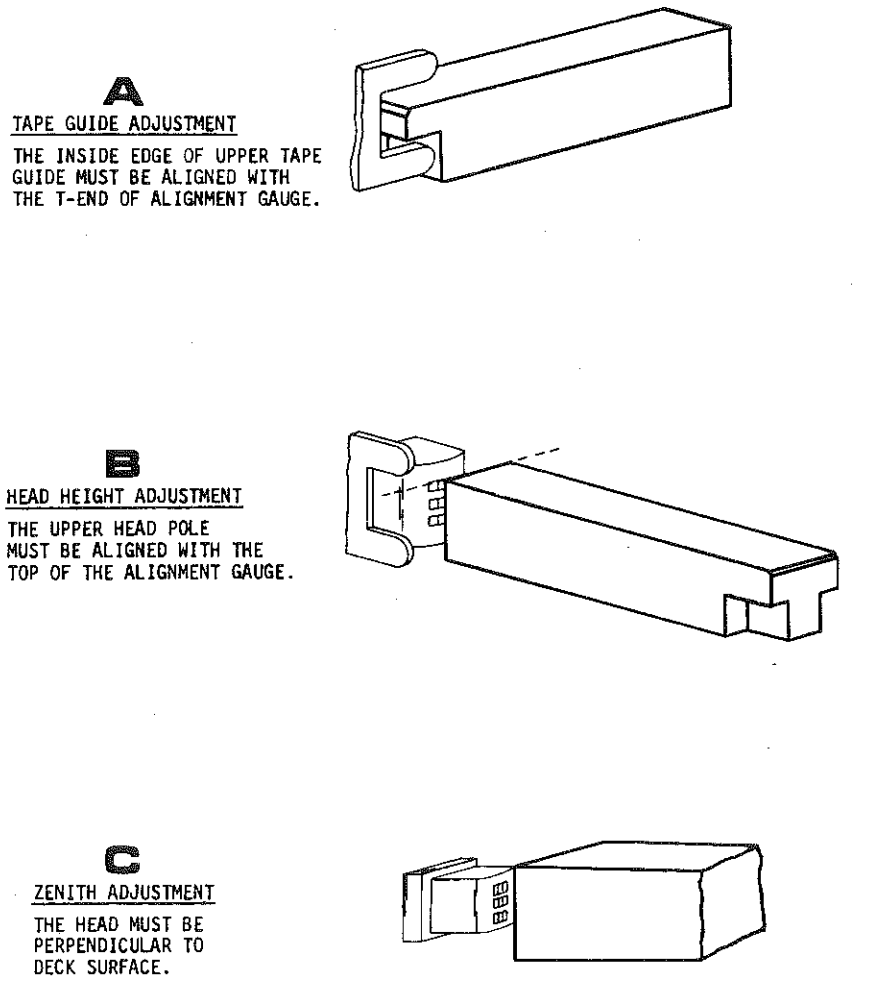

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FIGURE 5–5. HEAD AND TAPE GUIDE ADJUSTMENTS

5–55. If adjustment is required, refer to Figure 5–6 and loosen the appropriate head height/zenith lock–screw.

5–56. Refer to Figure 5–6 and adjust the appropriate front and rear head height/zenith adjustment screws as required to obtain the proper head height. The height/zenith screws must be adjusted equally to retain the zenith adjustment.

5–57. Secure the head height/zenith lock–screw.

5–58. For playback only cartridge machines, the top of the dummy head must be aligned with the top of the playback head. For record/playback units, the top of the record head must be aligned with the top of the playback head. Visually inspect the tape head heights. If required, adjust the dummy head or record height as required. Refer to Figure 5–6 for the location of the dummy/record head height/zenith adjustment screws.

5–59. **Head Zenith Adjustment Procedure.** To adjust the playback, record, or dummy head zenith, proceed as follows:

5–60. Refer to Figure 5–5C and check the playback or record head zenith. The head must be perpendicular to the deck surface.

5–61. If adjustment is required, refer to Figure 5–6 and loosen the appropriate head height/zenith lock–screw.

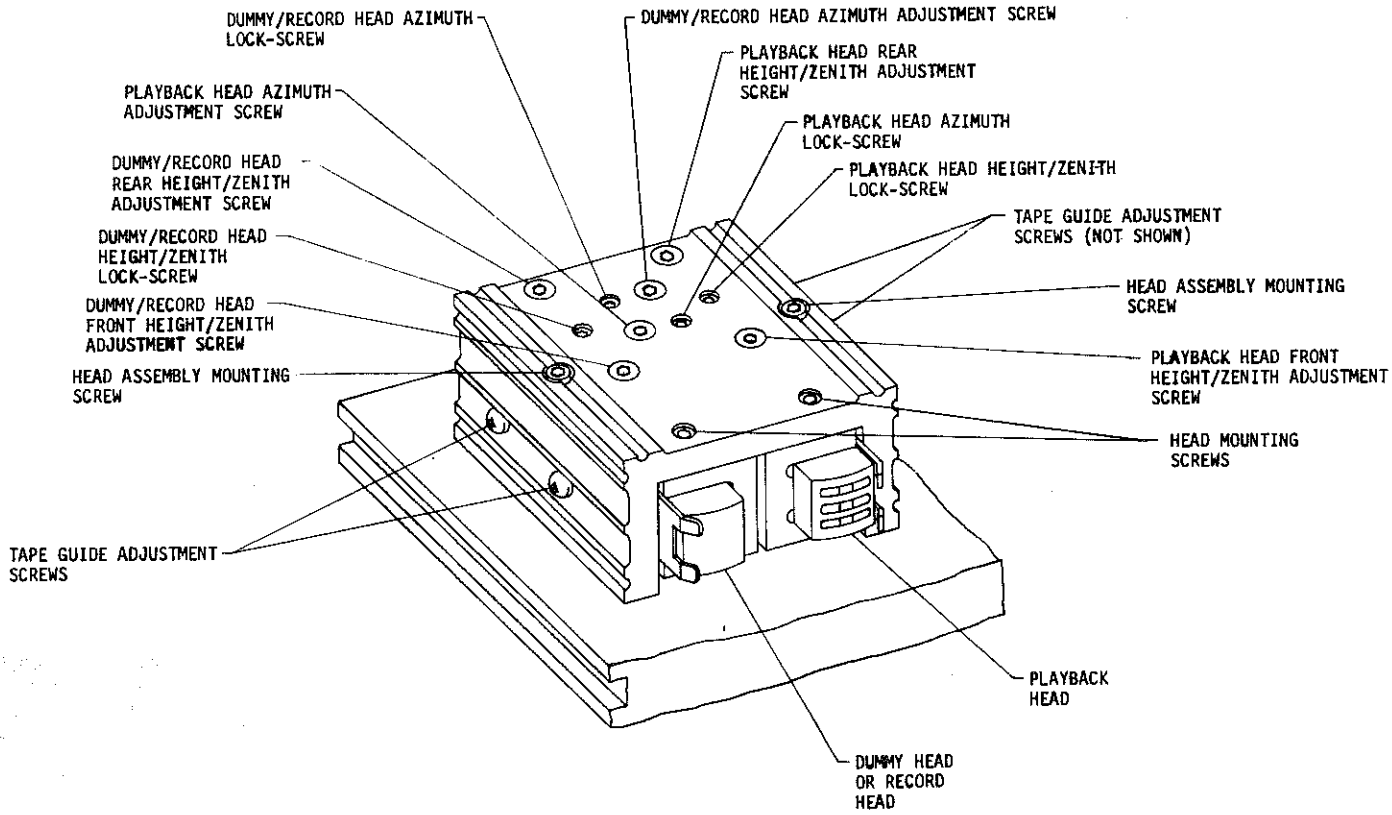

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FIGURE 5–6. HEAD ADJUSTMENT CONTROLS

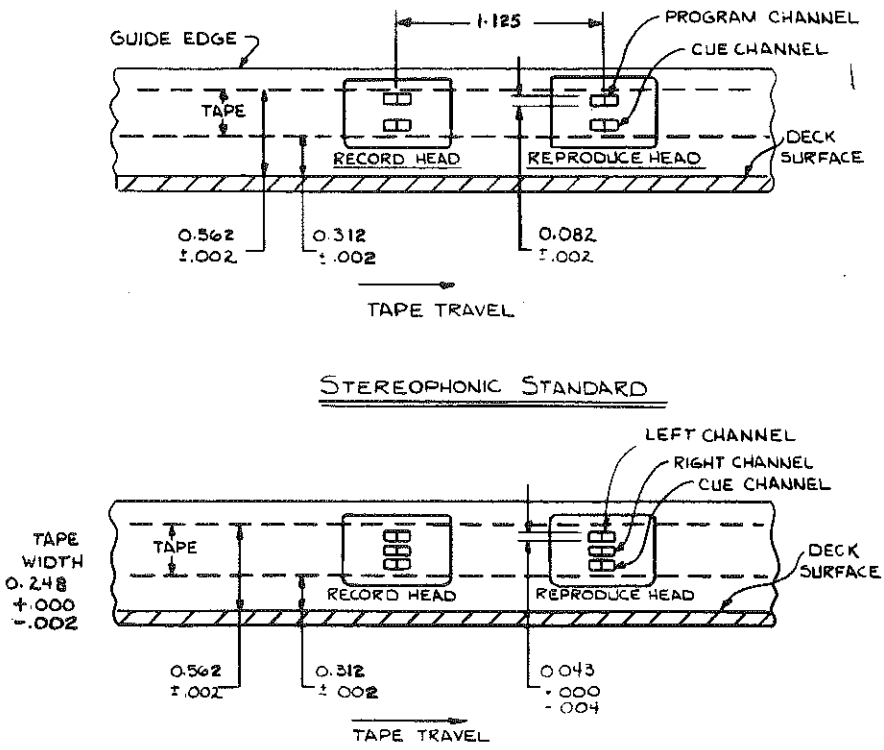

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FIGURE 5-7. HEIGHT CARTRIDGE TAPE TRACKING

5-62. Refer to Figure 5-6 and adjust the appropriate head front or rear height/zenith screw to obtain the proper alignment.

5-63. Refer to the **Head Height Adjustment Procedure** and check the head height. If required, re-adjust the head height.

5-64. Repeat the procedure until the head zenith and the head height is properly adjusted.

5-65. Secure the head height/zenith lock-screw.

5-66. For playback only cartridge machines, repeat the procedure for the dummy head. Refer to Figure 5-6 for the location of the dummy head height/zenith adjustment screws.

5-67. **Playback Head Azimuth Adjustment Procedure.** To adjust the playback head azimuth, proceed as follows:

5-68. Disconnect the cartridge machine primary power.

5-69. Demagnetize the playback head, the dummy/record head, and all surrounding ferrous components.

5-70. Refer to the OUTPUT LEVEL ADJUSTMENT procedure (located in the ELECTRICAL ADJUSTMENT procedures) and calibrate the cartridge deck for the desired output level.

5-71. Refer to Figure 2-3 and disable the phase correction circuitry.

5–72. Connect the oscilloscope to cartridge deck LEFT channel output receptacle J405.

5–73. Refer to Figure 5–6 and loosen the playback head azimuth lock–screw.

5–74. Apply power to the cartridge machine.

5–75. Insert the reproduce alignment test tape into the cartridge deck and reproduce the 12.5 kHz test tone.

5–76. Refer to Figure 5–6 and adjust the playback head azimuth screw for a maximum peak–to–peak voltage indication.

5–77. Secure the playback head azimuth lock–screw.

5–78. Disconnect power from the cartridge machine, remove the test equipment, and program the phase correction circuitry as required.

5–79. **Record Head Azimuth Adjustment Procedure.** To adjust the record head azimuth, proceed as follows:

5–80. Disconnect the cartridge machine primary power.

5–81. Demagnetize the record head, playback head, and all surrounding ferrous components.

5–82. Refer to the OUTPUT LEVEL ADJUSTMENT procedure (located in the ELECTRICAL ADJUSTMENT procedures) and calibrate the cartridge deck for the desired output level.

5–83. Connect the audio generator to the LEFT channel input on the record preamplifier module.

5–84. Connect the oscilloscope to the LEFT channel output on the audio module.

5–85. Refer to Figure 5–6 and loosen the record head azimuth lock–screw.

5–86. Apply power to the cartridge machine.

5–87. Adjust the audio generator for a 12.5 kHz output at 0 dBm.

5–88. Operate the record/playback unit in the record mode and begin recording the 12.5 kHz tone.

5–89. Refer to Figure 5–6 and adjust the record head azimuth screw for a maximum peak–to–peak voltage indication.

5–90. Secure the record head azimuth lock–screw.

5–91. Disconnect power from the cartridge machine and remove the test equipment.

5–92. **Playback Head Phase Response Adjustment Procedure.** (For Stereophonic Cartridge Machines Only). The playback phase adjustment involves the fine alignment of the playback head azimuth for maximum phase response. To adjust the playback head phase response, proceed as follows:

5–93. Disconnect the cartridge machine primary power.

5–94. Demagnetize the playback head, the dummy/record head, and all surrounding ferrous components.

5–95. Refer to the OUTPUT LEVEL ADJUSTMENT procedure (located in the ELECTRICAL ADJUSTMENT procedures) and calibrate the cartridge deck for the desired output level.

5–96. Refer to Figure 2–3 and disable the phase correction circuitry.

5–97. Connect an oscilloscope to the LEFT and RIGHT channel output receptacles J405 and J406 as shown in Figure 5–8.

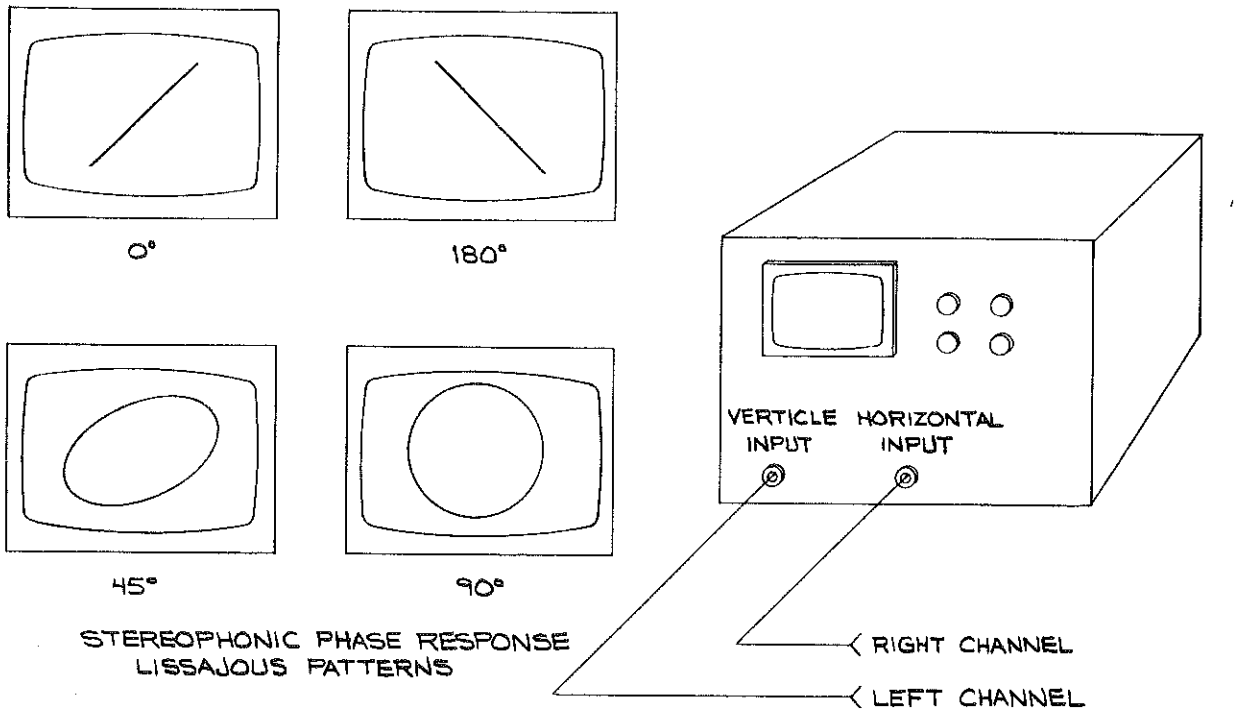

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FIGURE 5-8. STEREOPHONIC PHASE RESPONSE LISSAJOUS PATTERNS

5-98. Refer to Figure 5-6 and loosen the playback head azimuth lock-screw.

5-99. Apply power to the cartridge machine.

5-100. Operate the oscilloscope for lissajous display of inputs.

5-101. Insert the reproduce alignment test tape into the cartridge deck and reproduce the 12.5 kHz test tone.

5-102. Refer to Figure 5-6 and adjust the playback head azimuth screw for a 0° lissajous pattern (refer to Figure 5-8).

5-103. Secure the playback head azimuth lock-screw.

5-104. Disconnect power from the cartridge machine, remove the test equipment, and program the phase correction circuitry as required.

5-105. **Record Phase Adjustment Procedure.** The record phase adjustment involves the fine alignment of the record head azimuth for maximum phase response. To adjust the record head phase response, proceed as follows:

5-106. Disconnect the cartridge machine primary power.

5-107. Demagnetize the record head, the playback head, and all surrounding ferrous components.

5-108. Refer to the OUTPUT LEVEL ADJUSTMENT procedure (located in the ELECTRICAL ADJUSTMENT procedures) and calibrate the cartridge deck for the desired output level.

5–109. Refer to Figure 2–3 and disable the phase correction circuitry.

5–110. Connect the audio generator to the LEFT and RIGHT channel input receptacles on the record preamplifier module.

5–111. Connect the oscilloscope to the LEFT and RIGHT channel output receptacles on the audio module.

5–112. Refer to Figure 5–6 and loosen the record head azimuth lock–screw.

5–113. Apply power to the cartridge machine.

5–114. Operate the oscilloscope for a lissajous display of inputs.

5–115. Adjust the audio generator for a 12.5 kHz output at 0 dBm.

5–116. Operate the record/playback unit in the record mode and begin recording the 12.5 kHz tone.

5–117. Refer to Figure 5–6 and adjust the record head azimuth screw for a 0° lissajous pattern (refer to Figure 5–8).

5–118. Secure the record head azimuth lock–screw.

5–119. Disconnect power from the cartridge machine, remove the test equipment, and program the phase correction circuitry as required.

5–120. **ELECTRICAL ADJUSTMENTS.**

5–121. The following text provides electrical adjustment procedures for all controls associated with the PT–90 cartridge machines. The procedures are presented in the following order:

A. PLAYBACK ADJUSTMENTS.

1. Output Level Adjustment.
2. Playback Equalization Adjustment.
3. Phase Bias Adjustment.
4. Phase Distortion Adjustment.
5. Phase Display Adjustment.
6. Cue Sensitivity Adjustment.
7. FSK Frequency Adjustment.

B. MOTOR AND SOLENOID ADJUSTMENTS.

1. Motor Drive–Pulse Adjustment.
2. Solenoid Current Adjustment.

C. RECORD ADJUSTMENTS.

1. Digital–to–Analog Converter Alignment.
2. Analog–to–Digital Converter Alignment.
3. Distortion Adjustment.
4. Low Frequency Equalization.
5. Cue Bias Level Adjustment.

6. FSK/External Cue Audio Level Adjustment.
7. Cue Tone Record Level Adjustments.
8. Meter Calibrations.

5–122. The following equipment is required for the electrical adjustment procedures:

A. Frequency Counter.

B. Calibrated Oscilloscope, 5 MHz Bandwidth, Dual Channel with Lissajous Display of Inputs.

C. DC Voltmeter.

D. VU Meter (or decibel calibrated voltmeter).

E. Extender Circuit Board and Ribbon Cable Assemblies:
50–Pin Assembly (BE P/N 950–0105)
60–Pin Assembly (BE P/N 950–0106)

F. Stereophonic Reproduce Alignment Test Tape (BE P/N 800–1005).
Monophonic Reproduce Alignment Test Tape (BE P/N 800–1005–001).

G. Insulated Non–Metallic Adjustment Tool.

H. Cue Tone Calibration Cartridge (BE P/N 800–1095).

I. Audio Signal Generator (audio range: 20 Hz to 20 kHz).

J. Audio Analyzer.

5–123. **PLAYBACK ADJUSTMENTS.**

5–124. **OUTPUT LEVEL ADJUSTMENT.** Left channel level control R40 and right channel level control R43 on the audio module adjust the output level of the cartridge machine. The output level control(s) are adjusted as follows.

5–125. **Procedure.** To adjust the cartridge deck output level, proceed as follows:

5–126. Disconnect the cartridge machine primary power and remove the audio playback module.

5–127. Refer to Figure 2–3 and enable the phase correction circuitry (stereophonic models only).

5–128. Refer to Figure 2–3 and disable the noise reduction circuitry.

5–129. Re–install the audio playback module.

5–130. Connect the VU meter to the LEFT channel output on the audio module.

5–131. Apply power to the cartridge machine.

5–132. Insert the reproduce alignment test tape into the deck and reproduce the operating level portion of the test tape.

5–133. Refer to Figure 5–9B and adjust **LEFT LEVEL** control R40 for the desired output level.

5–134. For stereophonic cartridge machines, repeat the procedure for the right channel. Refer to Figure 5–9B and adjust the right channel with **RIGHT LEVEL** control R43 for the desired level.

5–135. Disconnect the cartridge machine primary power, program the phase correction and noise reduction circuitry as desired, and remove the test equipment.

5–136. **PLAYBACK EQUALIZATION ADJUSTMENT.** Equalization controls R6, R11, R13, and R18 on the audio playback circuit board adjust the left channel and right channel playback response. The equalization circuits will require periodic adjustment to compensate for degraded audio response due to normal tape head wear. Adjustment of the equalization circuits will also be required when replacement components are installed in the circuit or when the complete audio module is replaced. The playback equalization circuitry is adjusted as follows.

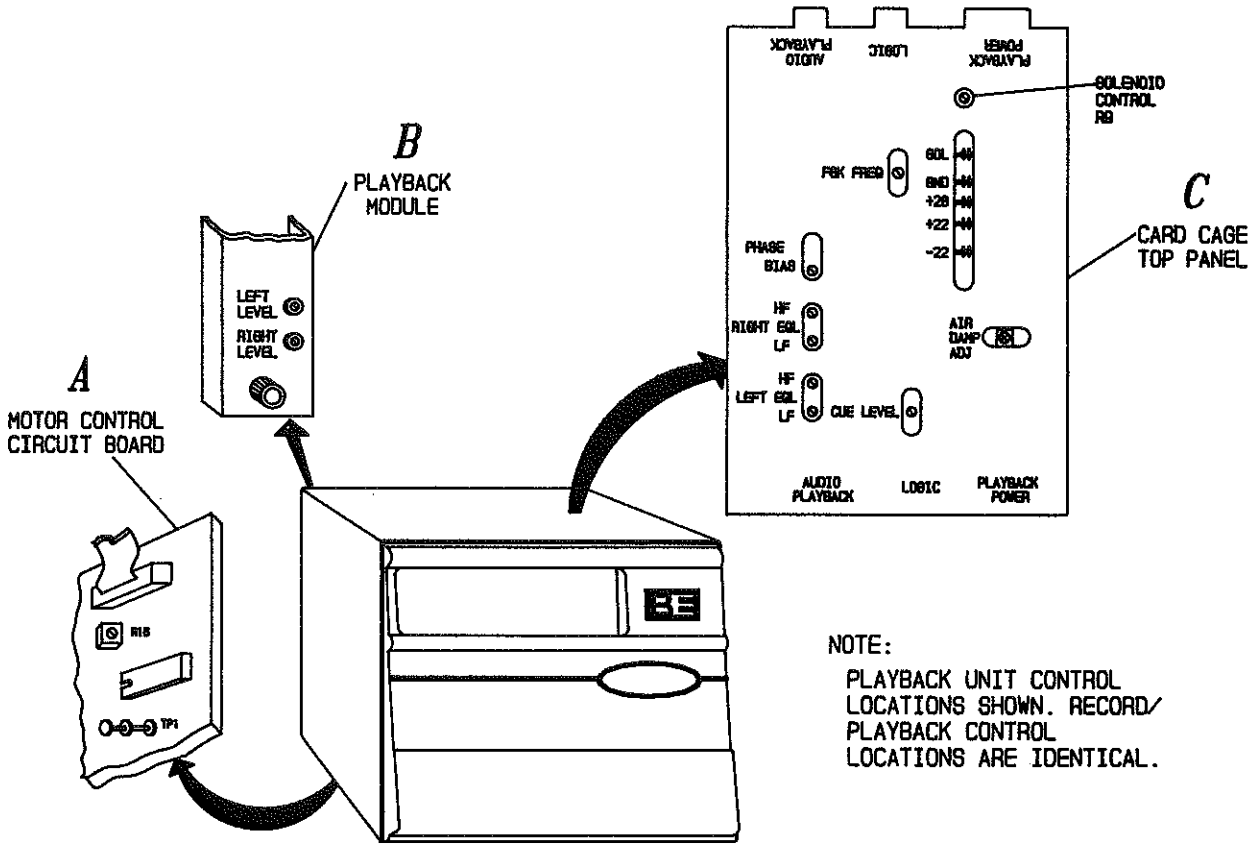

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FIGURE 5–9. PLAYBACK, LOGIC, AND MOTOR CONTROL CIRCUIT BOARD CONTROLS

5–137. **Procedure.** To adjust the equalization controls, proceed as follows:

5–138. Refer to the OUTPUT LEVEL ADJUSTMENT procedure in the preceding text and calibrate the cartridge deck for the desired level.

5–139. Disconnect the cartridge machine primary power and remove the top–panel.

5–140. Refer to Figure 2–3 and disable the noise reduction circuitry.

5–141. Connect the VU meter to the LEFT channel output on the audio module.

5–142. Insert the reproduce alignment tape and reproduce the test tones portion of the tape.

5–143. At the 50 Hz test tone, adjust **LEFT EQL LF** control R11 (refer to Figure 5–9C) until the VU meter indicates a level within –1 dB to 0 dB of the reference tone level.

5–144. At the 12.5 kHz test tone, adjust **LEFT EQL HF** control R6 (refer to Figure 5–9C) until the VU meter indicates the level of the reference tone.

5–145. For stereophonic cartridge machines, repeat the procedure for the right channel. Refer to Figure 5–9C and adjust the right channel equalization with **RIGHT EQL LF** control R18 and **RIGHT EQL HF** control R13.

5–146. Disconnect the cartridge machine primary power, program the noise reduction circuitry as desired, and remove the test equipment.

5–147. **PHASE BIAS ADJUSTMENT.** Phase bias control R35 adjusts the phase correction circuitry for a maximum correction range with a minimum offset between the left and right channels. Due to the critical operation of the correction circuitry, phase bias adjustment is not recommended. Therefore, it is suggested the defective audio circuit board be returned to Broadcast Electronics, Inc. for repair or exchange. If shipment to the factory is impractical, contact the Broadcast Electronics Customer Service Department for a recommended adjustment procedure and a list of required equipment.

5–148. **PHASE DISTORTION ADJUSTMENT.** Potentiometers R29 and R140 on the audio playback circuit board adjust for minimum phase distortion. Due to the critical operation of the circuit, phase distortion adjustment is not recommended. Therefore, it is suggested the defective audio circuit board be returned to Broadcast Electronics, Inc. for repair or exchange. If shipment to the factory is impractical, contact the Broadcast Electronics Customer Service Department for a recommended adjustment procedure and a list of required equipment.

5–149. **PHASE DISPLAY ADJUSTMENT.** Phase display control R77 on the audio playback circuit board calibrates the phase display. Due to the critical operation of the phase display circuitry, phase display adjustment is not recommended. Therefore, it is suggested the defective audio circuit board be returned to Broadcast Electronics, Inc. for repair or exchange. If shipment to the factory is impractical, contact the Broadcast Electronics Customer Service Department for a recommended adjustment procedure and a list of required equipment.

5–150. **CUE SENSITIVITY ADJUSTMENT.** Cue level control R10 on the logic circuit board adjusts the threshold level for the primary (1 kHz), secondary (150 Hz), tertiary (8 kHz) cue tone detection circuits, and the FSK decoder circuit. Adjustment of the cue sensitivity circuit will not be required unless replacement parts are installed in the circuit or the complete logic circuit board is replaced. The cue sensitivity circuit is adjusted as follows.

5–151. **Procedure.** To adjust the cue sensitivity control, proceed as follows:

5–152. Remove the top–panel.

5–153. Insert the cue tone calibration cartridge into the deck and reproduce the 8 kHz test tone (recorded at a –6 dB level).

5–154. Refer to Figure 5–9C and adjust **CUE LEVEL** control R10 until the **TER** indicator illuminates (refer to Figure 3–1).

5–155. Insert the cue tone calibration cartridge into the deck and reproduce the 1 kHz cue tone (recorded at a –6 dB level).

5–156. Refer to Figure 3–1 and ensure the **SEC** indicator is illuminated.

5–157. Insert the cue tone calibration cartridge into the deck and reproduce the 1 kHz cue tone (recorded at a –6 dB level).

5–158. Ensure deck operation terminates within 3 seconds.

5–159. Insert a pre–recorded FSK encoded tape into the deck and initiate playback operation.

5–160. Refer to Figure 3–1 and ensure the **DATA** indicator is illuminated.

5–161. Replace the top–panel.

5–162. **FSK FREQUENCY ADJUSTMENT.** FSK frequency control R45 on the logic circuit board adjusts the operating frequency of the FSK decoder circuit. The FSK decoder should be adjusted approximately once a year to ensure proper operation. The FSK decoder will also require adjustment when replacement components are installed in the circuit or the complete logic circuit board is replaced. The FSK decoder circuit is adjusted as follows.

5–163. **Procedure.** To adjust the FSK frequency control, proceed as follows:

5–164. Refer to the preceding text and perform the CUE SENSITIVITY ADJUSTMENT procedure.

5–165. Disconnect the cartridge machine primary power.

5–166. Remove the logic circuit board and the top–panel.

5–167. Insert the 50–pin extender circuit board into the logic module receptacle and connect the logic module to the extender circuit board.

5–168. Refer to Figure 5–10 and connect a frequency counter test probe to U10 pin 4.

5–169. Apply power to the cartridge machine.

5–170. Refer to Figure 5–10 and adjust **FSK FREQ** control R45 until the frequency counter indicates 3.25 kHz.

5–171. Insert a pre–recorded FSK encoded tape into the deck and initiate playback operation.

5–172. Refer to Figure 3–1 and ensure the **DATA** indicator is illuminated.

5–173. Disconnect the cartridge machine primary power.

5–174. Remove all test equipment and replace the logic circuit board and the top–panel.

5–175. **MOTOR AND SOLENOID ADJUSTMENTS.**

5–176. **MOTOR DRIVE–PULSE ADJUSTMENT.** Motor control potentiometer R16 on the motor control circuit board calibrates the duty cycle of the motor drive–pulse. Adjustment of the motor control circuit is not required unless replacement components are installed in the circuit or the complete motor control circuit board is replaced. The motor drive–pulse circuit is adjusted as follows.

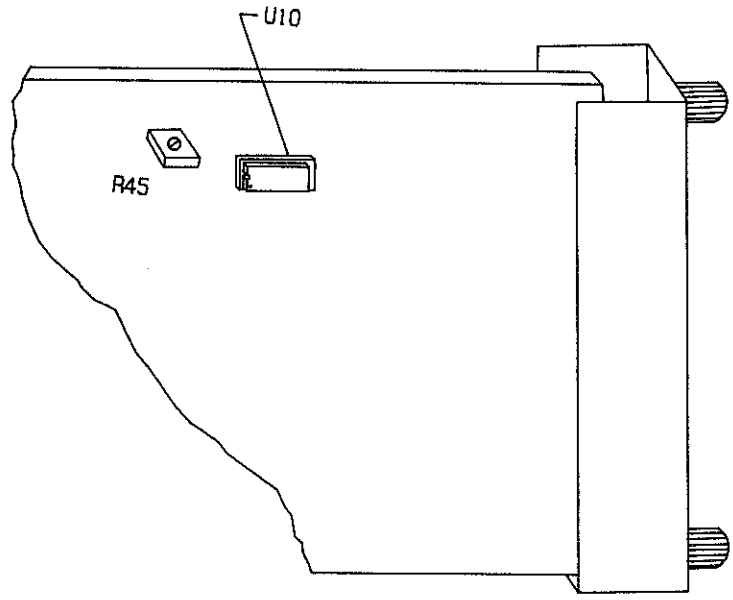

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FIGURE 5–10. LOGIC CIRCUIT BOARD CONTROLS

5–177. **Procedure.** To adjust the motor drive–pulse, proceed as follows:

5–178. Disconnect the cartridge machine primary power.

5–179. Refer to Figure 5–9A and connect an oscilloscope test probe to TP1 on the motor control circuit board. Adjust the oscilloscope as follows:

A. Input: 1 Meg Ohm
B. Mode: Triggered
C. Vertical Sensitivity: 1V/Div
D. Horizontal Rate: 0.5 ms/Div

5–180. Apply power to the cartridge machine.

5–181. Momentarily depress the **STOP** switch/indicator to operate the unit to the motor maintenance mode. The motor will operate for approximately 90 seconds.

5–182. Refer to Figure 5–9A and adjust motor drive–pulse control R16 until the front–panel **SVO** indicator just illuminates, then adjust R16 to extinguish the **SVO** indicator and to produce the oscilloscope waveform presented in Figure 5–11.

5–183. Disconnect the cartridge machine primary power.

5–184. Remove the test equipment.

5–185. **SOLENOID CURRENT ADJUSTMENT.** Solenoid control R9 on the power supply circuit board adjusts the solenoid current. Solenoid current adjustment is not required unless replacement components are installed in the circuit or the complete power supply circuit board is replaced. The solenoid control circuit is adjusted as follows.

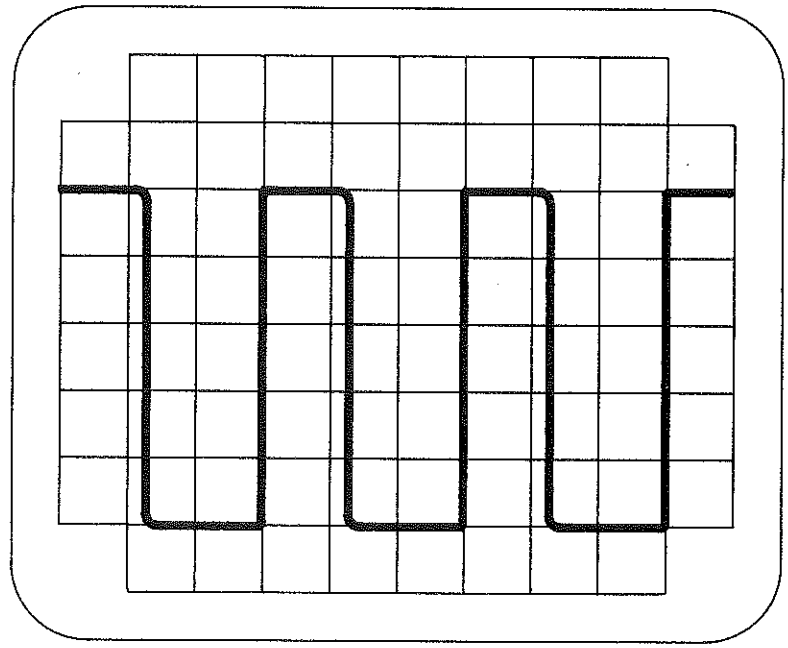

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FIGURE 5–11. MOTOR DRIVE–PULSE DUTY CYCLE

5–186. **Procedure.** To adjust the solenoid current, proceed as follows:

5–187. Disconnect the cartridge machine primary power. Remove the top–panel and allow the solenoid to cool to room temperature.

5–188. Refer to Figure 5–9C and connect a voltmeter between test points TP5 (SOL) and TP4 (GND).

5–189. Apply power to the cartridge machine.

5–190. Insert a blank tape into the deck and initiate deck operation.

5–191. Refer to Figure 5–9C and adjust solenoid control R9 until the voltmeter indicates +12V dc.

5–192. Disconnect the cartridge machine primary power.

5–193. Remove the test equipment and replace the top–panel.

5–194. **RECORD ADJUSTMENTS.**

5–195. **DIGITAL–TO–ANALOG CONVERTER ALIGNMENT.** Potentiometer R22 on the CPU module calibrates the Digital–to–Analog converter. Calibration of the digital–to–analog converter is not required unless replacement components are installed in the circuit or the complete CPU module is replaced. The analog–to–digital converter is calibrated as follows.

5–196. **Procedure.** To calibrate the digital–to–analog converter, proceed as follows:

5–197. Disconnect the cartridge machine primary power and remove the CPU module.

5–198. Insert the 60–pin extender circuit board assembly into the CPU module receptacle and connect the CPU module to the extender circuit board.

5–199. Refer to Figure 5–12 and connect the voltmeter to digital–to–analog converter calibration test point TP1.

5–200. Apply power to the cartridge machine.

5–201. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to MAN and insert a bulk erased tape cartridge into the deck.

5–202. Configure the unit to the Analog–to–Digital converter alignment mode by operating the **FCTN** switch until the tape time/function display indicates 0000.

5–203. Refer to Figure 5–12 and adjust D/A converter calibration control R22 until the voltmeter indicates +5.0 volts dc.

5–204. Disconnect power from the cartridge machine, remove the test equipment, and replace the CPU module.

5–205. **ANALOG–TO–DIGITAL CONVERTER CALIBRATION.** Left channel calibration control R12 and right channel calibration control R17 on the CPU module align the record/playback unit analog–to–digital converter. Calibration of the analog–to–digital converter is not required unless replacement components are installed in the circuit, the complete CPU module is replaced, or the playback reference level is changed. The analog–to–digital converter is calibrated as follows.

5–206. **Procedure.** To calibrate the analog–to–digital converter, proceed as follows:

5–207. Operate the rear–panel power switch to On.

5–208. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to MAN.

5–209. Select a normal (160 nWb/m) or elevated (250 nWb/m) level reproduce alignment tape for the calibration procedure as directed by the type of tapes in the station library. Insert the reproduce alignment tape into the unit.

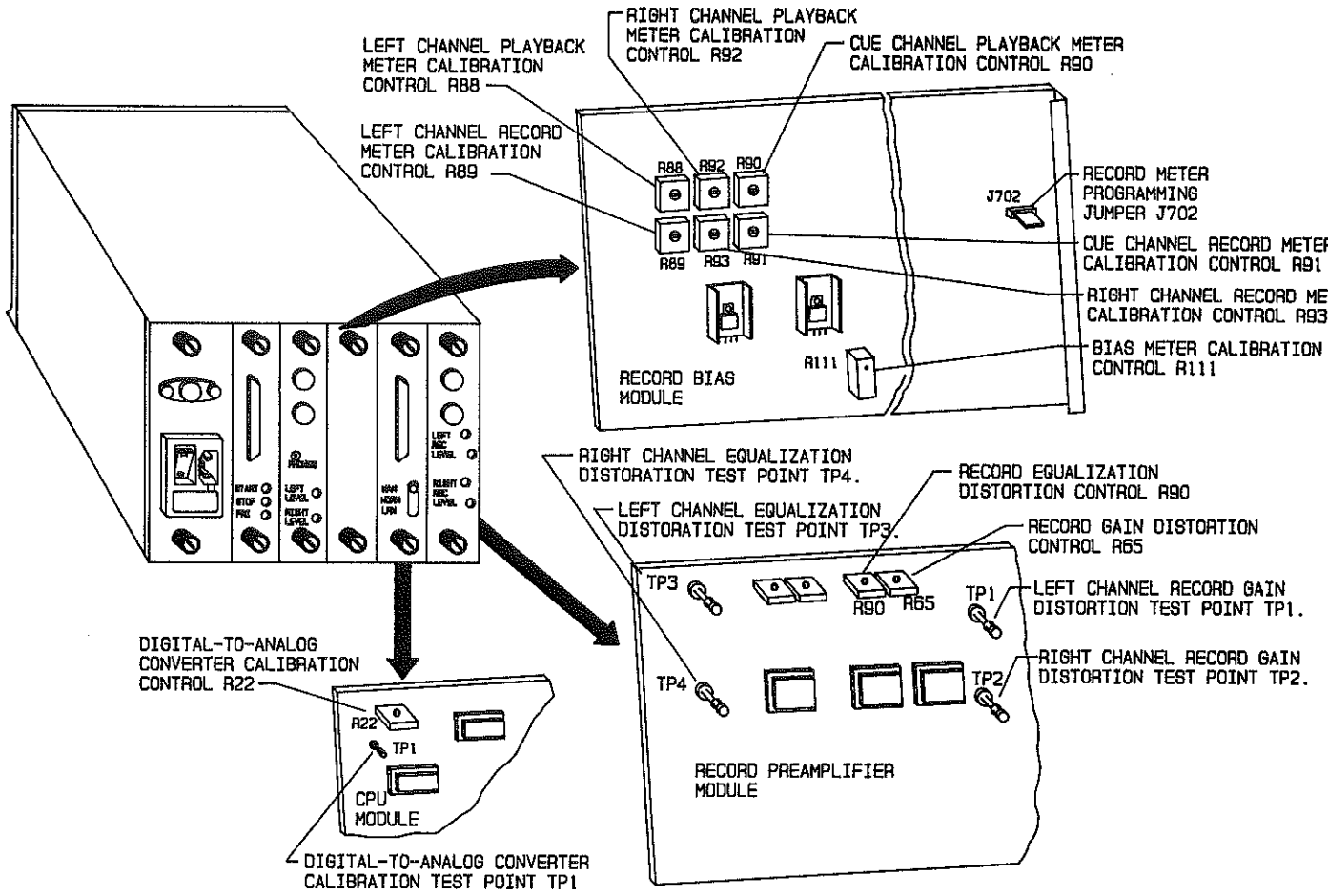

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FIGURE 5–12. RECORD/PLAYBACK UNIT INTERNAL RECORD CONTROLS

5–210. Configure the unit to the Analog–to–Digital converter alignment mode by operating the **FCTN** switch until the tape time/function display indicates 0000.

5–211. Reproduce the alignment tape 1 kHz operating level tone.

5–212. Refer to Figure 5–13 and adjust L A/D control R12 until the the first and second digits of the tape time/function display indicate 32__.

5–213. Repeat the procedure for the right channel. Refer to Figure 5–13 and adjust the right channel with R A/D control R17 until the third and fourth digits of the tape time/function display indicate __32.

5–214. Remove the reproduce alignment tape and operate the rear–panel **MAN/NORM/LRN** switch to the desired position.

5–215. **DISTORTION ADJUSTMENT.** Record gain distortion control R65 and record equalization distortion control R90 on the record preamplifier module nulls the audio circuitry total–harmonic–distortion. Distortion adjustment is not required unless VCA modules U6, U7, U12, or U13 are replaced or the complete record preamplifier module is replaced. The audio circuitry distortion is nulled as follows.

5–216. **Procedure.** To null the audio circuitry distortion, proceed as follows:

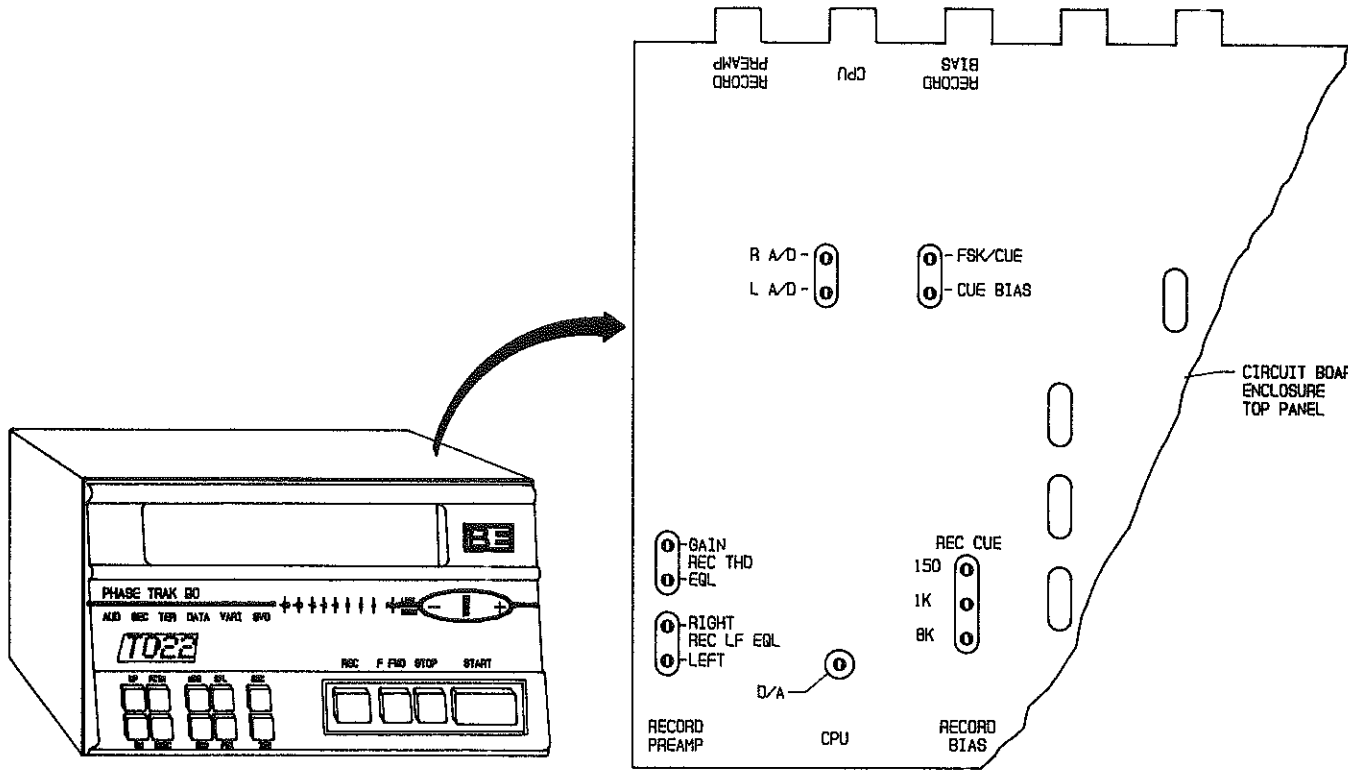

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FIGURE 5–13. RECORD/PLAYBACK UNIT RECORD CONTROLS

5–217. Disconnect the cartridge machine primary power and remove the record preamplifier module.

5–218. Insert the 50–pin extender circuit board assembly into the record preamplifier module receptacle and connect the record preamplifier module to the extender circuit board.

5–219. Connect the audio signal generator to the LEFT and RIGHT channel inputs on the record preamplifier module.

5–220. Null the record gain distortion as follows:

A. Refer to Figure 5–12 and connect the audio analyzer between left channel record gain distortion test point TP1 on the record preamplifier module and chassis ground.

B. Apply power to the cartridge machine.

C. Adjust the audio generator for a 1 kHz output at a level to illuminate the **LEFT REC LEVEL** and **RIGHT REC LEVEL** indicators.

D. Refer to Figure 5–12 and adjust record gain distortion control R65 for a minimum audio analyzer indication.

E. Refer to Figure 5–12 and connect the audio analyzer between right channel record gain distortion test point TP2 on the record preamplifier module and chassis ground.

F. Ensure the analyzer indication is less than 0.25%. If the analyzer indication is greater than 0.25%, refer to Figure 5–12 and adjust record gain distortion control R65 for a minimum audio analyzer indication. Repeat the procedure and ensure the left and right channel distortion is less than 0.25%.

5–221. Disconnect the cartridge machine primary power.

5–222. Null the record equalization distortion as follows:

A. Refer to Figure 5–12 and connect the audio analyzer between left channel record equalization distortion test point TP3 on the record preamplifier module and chassis ground.

B. Apply power to the cartridge machine.

C. Adjust the audio generator for a 12.5 kHz output at a level to illuminate the **LEFT REC LEVEL** and **RIGHT REC LEVEL** indicators.

D. Refer to Figure 5–12 and adjust record equalization distortion control R90 for a minimum audio analyzer indication.

E. Refer to Figure 5–12 and connect the audio analyzer between right channel record equalization test point TP4 on the record preamplifier module and chassis ground.

F. Ensure the analyzer indication is less than 0.25%. If the analyzer indication is greater than 0.25%, refer to Figure 5–12 and adjust record equalization distortion control R90 for a minimum audio analyzer indication.

G. Repeat the procedure and ensure both the left and right channel distortion is less than 0.25%.

5–223. Disconnect the cartridge machine primary power.

5–224. Remove all test equipment and replace the record preamplifier module.

5–225. **RECORD LOW FREQUENCY EQUALIZATION.** Left channel low frequency equalization control R47 and right channel low frequency equalization control R48 adjust the audio equalization. Adjustment of the equalization circuitry is not required unless replacement components are installed in the circuit or the complete record preamplifier module is replaced. The record low frequency equalization is adjusted as follows.

5–226. **Procedure.** To adjust the record low frequency equalization, proceed as follows.

5–227. Disconnect the cartridge machine primary power.

5–228. Connect the external VU meter to the LEFT channel audio output on the audio module.

5–229. Apply power to the cartridge machine.

5–230. Configure the unit internal test oscillator to generate a 50 Hz tone as follows:

A. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to MAN.

B. Operate the **FCTN** switch until the tape time/function display indicates – OFF.

C. Operate the **UP** and **DN** switches as required until the tape time/function display indicates – 50.

5–231. Operate the unit to the record mode and begin recording the 50 Hz tone.

5–232. Refer to Figure 5–13 and adjust **LEFT REC LF EQL** control R47 for the unit playback output level as indicated by the external VU meter.

5–233. Refer to Figure 5–13 and adjust **RIGHT REC LF EQL** control R48 for the unit playback output level as indicated by the external VU meter.

5–234. Disconnect power from the cartridge machine and remove all test equipment.

5–235. **CUE BIAS LEVEL ADJUSTMENT.** Potentiometer R30 on the record bias module adjusts the cue bias level. Adjustment of the cue bias is not required unless replacement components are installed in the circuit or the complete record bias module is replaced. The cue bias level is adjusted as follows.

5–236. **Procedure.** To adjust the cue bias level, proceed as follows:

5–237. Disconnect the cartridge machine primary power.

5–238. Refer to Figure 2–7 in SECTION II, INSTALLATION and perform the following:

A. Activate the cue bias by connecting a jumper between pin 4 and pin 8 on record remote control receptacle J802.

B. Connect the audio signal generator to remote control receptacle J802 pin 10.

5–239. Refer to Figure 2–6 in SECTION II, INSTALLATION and connect the oscilloscope to the cue channel audio output on playback remote control receptacle J308.

5–240. Apply power to the cartridge machine.

5–241. Adjust the audio generator for a 1 kHz output at –10 dBm.

5–242. Operate the unit in the playback mode and begin recording the 1 kHz cue tone.

5–243. Refer to Figure 5–13 and adjust **CUE BIAS** level control R30 for a maximum peak–to–peak 1 kHz waveform without distortion.

5–244. Disconnect power from the cartridge machine, remove all test equipment, and remove the jumper from record remote control receptacle J802.

5–245. **FSK/EXTERNAL CUE AUDIO LEVEL ADJUSTMENT.** Potentiometer R16 on the record bias module controls the FSK and external cue audio level. The FSK/cue audio level control will require adjustment only when the external FSK/cue audio source is changed. The FSK/external cue audio level is adjusted as follows.

5–246. **Procedure.** To adjust the FSK/external cue audio level, proceed as follows:

5–247. Disconnect the cartridge machine primary power.

5–248. Refer to Figure 2–7 in SECTION II, INSTALLATION and perform the following:

A. Activate the cue bias by connecting a jumper between pin 4 and pin 8 on remote control receptacle J802.

B. Connect the audio signal generator to remote control receptacle J802 pin 10.

5–249. Refer to Figure 2–6 in SECTION II, INSTALLATION and connect the external VU meter to the cue channel audio output on playback remote control receptacle J308.

5–250. Apply power to the cartridge machine and insert a bulk erased tape cartridge into the deck.

5–251. Adjust the audio generator for a 1 kHz output at –10 dBm.

5–252. Operate the unit in the playback mode and begin recording the 1 kHz cue tone.

5–253. Refer to Figure 5–13 and adjust **FSK/CUE** level control R16 for a –10 dBm external VU meter indication.

5–254. Disconnect power from the cartridge machine, remove all test equipment, and remove the jumper from record remote control receptacle J802.

5–255. **CUE TONE RECORD LEVEL ADJUSTMENTS.** Primary cue tone control R53, secondary cue tone control R63, and tertiary cue tone control R54 adjust the individual cue tone record levels. Adjustment of the cue tone levels is not required unless replacement components are installed in the circuit or the complete record bias module is replaced. The cue tone record levels are adjusted as follows.

5–256. **1 kHz Cue Tone Record Level Adjustment.** To adjust the 1 kHz cue tone level, proceed as follows:

5–257. Measure the NAB 1 kHz cue tone level standard as follows:

A. Disconnect the cartridge machine primary power.

B. Refer to Figure 2–6 in SECTION II, INSTALLATION and connect the oscilloscope to the cue channel audio output on playback remote control receptacle J308.

C. Apply power to the cartridge machine.

D. Insert the NAB 1 kHz cue tone reference level test tape into the deck.

E. Reproduce the 1 kHz cue tone and record the peak–to–peak voltage indication _____.

F. Terminate reproduce operations and remove the NAB cue tone test tape.

5–258. Insert a bulk erased tape cartridge into the deck and operate the unit in the playback mode.

5–259. Continuously depress and release the **PRI** switch/indicator and observe the oscilloscope indication.

5–260. Refer to Figure 5–13 and adjust 1K cue tone level control R53 for the recorded NAB standard level.

5–261. Disconnect the cartridge machine primary power and remove all test equipment.

5–262. **150 Hz Cue Tone Record Level Adjustment.** To adjust the 150 Hz cue tone level, proceed as follows:

5–263. Measure the NAB 150 Hz cue tone level standard by performing the level measurement procedure described in the **1 kHz Cue Tone Record Level Adjustment** procedure. Record the peak–to–peak voltage indication _____.

5–264. Insert a bulk erased tape cartridge into the deck and operate the unit in the playback mode.

5–265. Continuously depress the **SEC** switch and observe the oscillo–scope indication.

5–266. Refer to Figure 5–13 and adjust 150 Hz cue tone level control R63 for the recorded NAB standard level.

5–267. Disconnect the cartridge machine primary power and remove all test equipment.

5–268. **8 kHz Cue Tone Record Level Adjustment.** To adjust the 8 kHz cue tone level, proceed as follows:

5–269. Measure the NAB 8 kHz cue tone level standard by performing the level measurement procedure described in the **1 kHz Cue Tone Record Level Adjustment** procedure. Record the peak–to–peak voltage indication _____.

5–270. Insert a bulk erased tape cartridge into the deck and operate the unit in the playback mode.

5–271. Continuously depress the **TER** switch and observe the oscilloscope indication.

5–272. Refer to Figure 5–13 and adjust 8 kHz cue tone level control R54 for the recorded NAB standard level.

5–273. Disconnect the cartridge machine primary power and remove all test equipment.

5–274. **METER CALIBRATION.** Potentiometers R88 through R93 and R111 calibrate the PT–90 record/playback unit front–panel VU meter. Calibration of the meter circuitry is not required unless replacement components are installed in the circuit or the complete record bias module is replaced. The front–panel VU meter is calibrated as follows.

5–275. **Playback Meter Calibrations.** To calibrate the playback VU meter parameters, proceed as follows:

5–276. Refer to the OUTPUT LEVEL ADJUSTMENT procedure in the preceding text and calibrate the cartridge machine for the desired output level.

5–277. Disconnect the cartridge machine primary power.

5–278. Connect the external VU meter to the LEFT channel audio output on the audio module.

5–279. Insert the 50–pin extender circuit board assembly into the record bias module receptacle and connect the record bias module to the extender circuit board.

5–280. Apply power to the cartridge machine.

5–281. Insert the reproduce alignment test tape into the deck and reproduce the 1 kHz tone.

5–282. Refer to Figure 5–12 and adjust left channel playback meter calibration control R88 until the front–panel VU meter left channel display is equal to the output level indicated on the external VU meter.

5–283. Disconnect the cartridge machine primary power and connect the external VU meter to the RIGHT channel output on the audio module.

5–284. Apply power to the cartridge machine and reproduce the 1 kHz test tone.

5–285. Refer to Figure 5–12 and adjust right channel playback meter calibration control R92 until the front–panel VU meter right channel display is equal to the output level indicated on the external VU meter.

5–286. Operate the **STOP** switch/indicator to illuminate the switch/indicator.

5–287. Insert the NAB 1 kHz cue tone reference level tape into the deck and reproduce the 1 kHz tone.

5–288. Operate the **MTR** switch/indicator to illuminate the switch/indicator.

5–289. Refer to Figure 5–12 and adjust cue channel playback meter calibration control R90 until the front–panel VU meter left channel display indicates 0 dB.

5–290. Disconnect the cartridge machine primary power, replace the record bias module, and remove all test equipment.

5–291. **Record Meter Calibrations.** To calibrate the record VU meter parameters, proceed as follows:

5–292. Disconnect the cartridge machine primary power.

5–293. Connect the external VU meter to the LEFT channel audio output on the audio module.

5–294. Insert the 50–pin extender circuit board assembly into the record bias module receptacle and connect the record bias module to the extender circuit board.

5–295. Refer to Figure 5–12 and program the meter circuitry for record monitoring by removing record meter program jumper J702.

5–296. Connect the audio signal generator to the LEFT channel audio input on the audio module.

5–297. Apply power to the cartridge machine.

5–298. Operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to MAN.

5–299. Operate the **FCTN** and **EXEC** switches until the tape time/function display indicates FL__.

5–300. Adjust the audio signal generator for a 1 kHz output at 0 dBm.

5–301. Insert a bulk erased tape into the deck and operate the unit to begin recording the 1 kHz tone.

5–302. Operate the **UP** and **DN** switches as required to obtain an external VU meter indication equal to the playback audio level.

5–303. Refer to Figure 5–12 and adjust left channel record meter calibration control R89 until the front–panel VU meter left channel display is equal to the output level indicated on the external VU meter.

5–304. Repeat the procedure for the right channel. Adjust the right channel using right channel record meter calibration control R93 (refer to Figure 5–12).

5–305. Disconnect the cartridge machine primary power.

5–306. Refer to Figure 5–12 and remove jumper J702 on the record bias module.

5–307. Operate the **MTR** switch/indicator to illuminate the switch/indicator.

5–308. Insert a bulk erased tape cartridge into the deck and operate the unit in the record mode.

5–309. Continuously depress and release the **PRI** switch/indicator and observe the front–panel VU meter left channel indication.

5–310. Refer to Figure 5–12 and adjust cue channel record meter calibration control R91 for a 0 dB left channel VU meter indication.

5–311. Disconnect the cartridge machine primary power, replace the record bias module, and remove all the test equipment.

5–312. **Record Bias Meter Calibration.** To calibrate the record bias meter parameter, proceed as follows:

5–313. Disconnect the cartridge machine primary power.

5–314. Insert the 50–pin extender circuit board assembly into the record bias module receptacle and connect the record bias module to the extender circuit board.

5–315. Apply power to the cartridge machine and operate the rear–panel **MAN/NORM/LRN** switch on the CPU module to LRN.

5–316. Insert a bulk erased tape cartridge into the deck and operate the unit in the LRN mode to establish a set of record compensation characteristics (refer to SECTION III, OPERATION).

5–317. When LRN mode operation is complete, operate the **REC** and **START** switch/indicators to illuminate the switch/indicators.

5–318. Operate the **MTR** switch/indicator to illuminate the switch/indicator.

5–319. Refer to Figure 5–12 and adjust bias meter calibration control R111 for a 0 dB right channel VU meter indication.

5–320. Disconnect the cartridge machine primary power, replace the record bias module, and operate the **MAN/NORM/LRN** switch to the desired position.

5–321. MECHANICAL PARTS REPLACEMENT PROCEDURES.

5–322. The following text provides mechanical parts replacement procedures. The procedures are presented in the following order.

A. Pressure Roller Replacement.

B. Head Replacement.

C. Motor Replacement.

5–323. The following equipment is required for the replacement procedures. Refer to the list as required for each procedure.

EQUIPMENT

A. No. 1 Phillips Screwdriver, 4 Inch (10.2 cm) Blade.

B. Needle–nose pliers.

C. Allen Wrenches (supplied with the cartridge machine).

5–324. **PRESSURE ROLLER REPLACEMENT PROCEDURE.** To replace a cartridge deck pressure roller, proceed as follows:

5–325. Disconnect the cartridge machine primary power.

5–326. Refer to Figure 5–1 and manually retract the solenoid plunger.

5–327. Remove the pressure roller E–ring, the pressure roller, and the nylon washers (refer to Figure 5–1).

5–328. Refer to Figure 5–1 and replace the washers, the pressure roller, and the pressure roller E–ring.

5–329. Check the pressure roller indentation by performing the PRESSURE ROLLER INDENTATION ADJUSTMENT procedure.

5–330. **HEAD REPLACEMENT.** To replace a tape head, proceed as follows:

5–331. Disconnect the cartridge machine primary power.

5–332. Loosen the head assembly mounting screws (refer to Figure 5–6) and remove the entire head assembly from the cartridge deck.

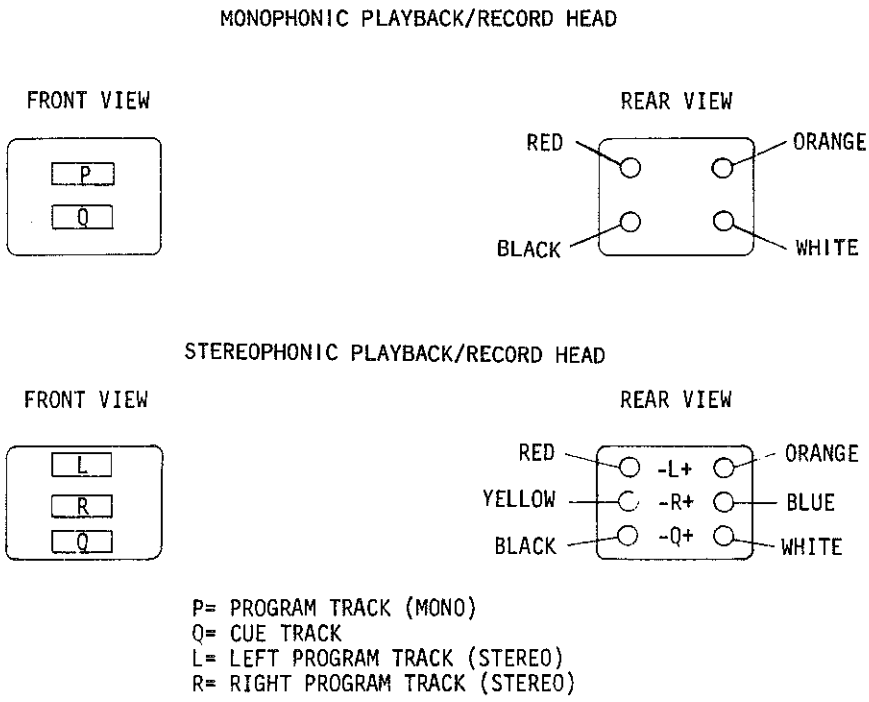
5–333. Refer to Figure 5–6 and loosen the defective tape head mounting screw.

5–334. Remove the defective head from the head assembly and disconnect the head leads.

5–335. Refer to Figure 5–14 and connect the head leads to the replacement head.

5–336. Firmly seat the replacement head into the head assembly and secure the mounting screw.

5–337. Replace the head assembly and secure the mounting screws.



597–9000–41

FIGURE 5–14. TAPE HEAD CONFIGURATIONS

5–338. Align the head by performing all the HEAD ADJUSTMENTS and associated ELECTRICAL ADJUSTMENT procedures.

5–339. **MOTOR REPLACEMENT.** To replace the cartridge machine motor, proceed as follows:

5–340. Disconnect the cartridge machine primary power.

5–341. Remove the cartridge machine top–panel and bottom–panel.

5–342. Place the cartridge machine on a side–panel.

5–343. Refer to the cartridge machine final assembly diagram in SECTION VII, DRAWINGS and disconnect motor power supply connector P601 from the motor control board (located near the motor).

5–344. Refer to Figure 5–2 and locate the motor mounting screws. While supporting the motor, remove the motor mounting screws and carefully remove the motor from the cartridge machine chassis.

CAUTION

CAUTION

EXERCISE CARE WHEN HANDLING THE CARTRIDGE MACHINE MOTOR TO AVOID DAMAGING THE BEARINGS. NEVER HANDLE THE MOTOR BY THE CAPSTAN SHAFT.

5–345. Carefully insert the new motor into the cartridge machine chassis and replace the motor mounting screws. Do not tighten the motor mounting screws at this time.

5–346. Reconnect motor power supply connector P601 to the motor control circuit board.

5–347. Align the motor by performing the MOTOR ALIGNMENT PROCEDURE and PRESSURE ROLLER INDENTATION ADJUSTMENT procedures described in the preceding text.

5–348. Replace the cartridge machine top–panel and bottom–panel.

5–349. **TROUBLESHOOTING.**

5–350. Low voltages are used throughout the PT–90 series cartridge machine playback and control circuitry. The power supply circuit board assembly contains primary ac line voltage. Therefore, do not perform any maintenance or troubleshooting procedures on the power supply circuit board with power energized. Troubleshooting with power energized is always considered hazardous and caution should be observed. Good judgment, care, and common sense must be practiced to prevent accidents.

5–351. The troubleshooting philosophy for the PT–90 series cartridge machines consists of isolating a problem to a specific circuit board. The problem may be isolated by referencing the following information and Tables 5–1 and 5–2 which present the PT–90 series cartridge machine troubleshooting.

TABLE 5–1. PT–90 CARTRIDGE MACHINE PLAYBACK OPERATION TROUBLESHOOTING (Sheet 1 of 2)

SYMPTOM	DEFECT
NO MOTOR OPERATION	1. Check the cartridge deck status switch. 2. Refer to Table 5–3 and troubleshoot the logic module. 3. Refer to Figure 5–15 and troubleshoot the motor control circuit board. 4. Check the cartridge machine motor.
NO DECK START OPERATION	1. Check front panel start switch/indicator S1. 2. Refer to Table 5–3 and troubleshoot the logic module. 3. Check integrated circuit IC–1 on the cartridge machine rear panel. 4. Check transistors Q1 and Q2 on the power supply module. 5. Check the deck solenoid.
NO DECK TERMINATION, MANUAL	1. Check front panel stop switch/indicator S2. 2. Refer to Table 5–3 and troubleshoot the logic module.
NO FAST FORWARD OPERATION	1. Check front panel fast forward switch/indicator S3. 2. Refer to table 5–3 and troubleshoot the logic module.

TABLE 5–1. PT–90 CARTRIDGE MACHINE PLAYBACK OPERATION TROUBLESHOOTING (Sheet 2 of 2)

SYMPTOM	DEFECT
NO AUDIO OUTPUT	1. Refer to Figure 5–16 and troubleshoot the audio module.
NO INTERNAL OPERATIONS (EXAMPLE: EOM, MUTE, CUE TONE ETC.)	1. Refer to Table 5–3 and troubleshoot the logic module.
NO PHASE CORRECTION DISPLAY OPERATION	1. Check integrated circuit U3B on the audio module. 2. Check integrated circuits U1 and DS7 on the front panel display circuit board.
NO TAPE TIME DISPLAY OPERATION	1. Refer to Table 5–3 and troubleshoot the logic module. 2. Check integrated circuits U2 and DS8 on the front panel display circuit board.

TABLE 5–2. PT–90 CARTRIDGE MACHINE RECORD OPERATION TROUBLESHOOTING (Sheet 1 of 2)

SYMPTOM	DEFECT
NO RECORD AUDIO	Refer to Figure 5–17.
NO PRIMARY/SECONDARY CUE TONE RECORD OPERATION	1. Primary Cue Tone: Check switch S4 on the front panel circuit board. Secondary Cue Tone: Check switch S1 on the front panel circuit board. 2. Refer to Figure 5–18.
NO TERTIARY CUE TONE RECORD OPERATION	1. Check switch S2 on the front panel circuit board. 2. Refer to Figure 5–19.
NO PLAYBACK/RECORD METER OPERATION	Refer to Figure 5–20.
NO CUE RECORD/PLAYBACK METER OPERATION	Refer to Figure 5–21.
NO BIAS METER OPERATION	Refer to Figure 5–22.

TABLE 5–2. PT–90 CARTRIDGE MACHINE RECORD OPERATION TROUBLESHOOTING
(Sheet 2 of 2)

SYMPTOM	DEFECT
NO 50 Hz TO 8 kHz TEST TONE OPERATION	Refer to Figure 5–23.
NO 12 kHz TO 16 kHz TEST TONE OPERATION	Refer to Figure 5–24.
NO FSK ENCODING OPERATION	Refer to Figure 5–25.
NO RECORD MODE OPERATION	1. Check record switch S4. 2. Check integrated circuits U1, U2, and U4 on the CPU module.
PLAYBACK MODE FUNCTIONS OPERATIONAL – NO RECORD FUNCTIONS	1. Reset the microprocessor. 2. Check integrated circuits U1 and U3 on the CPU module.
NO REMOTE CONTROL OPERATION	Check integrated circuit U1 on the CPU module.
RANDOM OR SCRAMBLED DISPLAY OF INFORMATION ON THE TAPE TIME/FUNCTION DISPLAY	Check integrated circuit U8 on the CPU module.

TABLE 5–3. LOGIC MODULE TROUBLESHOOTING.
(Sheet 1 of 2)

SYMPTOM	DEFECT
NO MOTOR OPERATION	1. Check integrated circuits U16A and U17A. 2. Check integrated circuit U12A.
NO DECK START OPERATION	1. Check for a HIGH at motor–at–speed status line P301 pin 14. 2. Check for a LOW at motor over–current status line P301 pin 15. 3. Check integrated circuits U25A, U19A, and U17B.
NO DECK TERMINATION, MANUAL	1. Check integrated circuits U21B and U25A.
NO DECK TERMINATION, PRIMARY CUE TONE	1. Ensure jumper J314 is installed in position 1–2. 2. Check integrated circuits U20C, U21B, and U12C.

TABLE 5–3. LOGIC MODULE TROUBLESHOOTING.
(Sheet 2 of 2)

SYMPTOM	DEFECT
	3. Check for a LOW at primary cue tone defeat control line P301 pin 7.
NO FAST FORWARD OPERATION	1. Check integrated circuits U23A and U22D.
NO EOM OPERATION	1. Ensure jumper J305 is installed for the correct cue tone. 2. Check integrated circuits U13A, U23B, and U22B.
NO MUTE OPERATION	1. Check integrated circuits U25C andU21D.
TAPE TIME DISPLAY CONTROL PROBLEMS (EXAMPLE: RESET, FREEZE ETC.)	1. Ensure jumper J306 is installed in the correct position for the desired operation. 2. Ensure jumper J309 is installed in the appropriate position for the desired operation. 3. Check P301 pin 43 for one Hz pulses. 4. Check integrated circuit U16F.
NO CUE TONE OPERATION (INCLUDES PRIMARY, SECONDARY, TERTIARY, AND FSK.)	1. Ensure jumper W3 is installed in the appropriate position. 2. Check integrated circuit U1.
NO INDIVIDUAL PRIMARY, SECONDARY, OR TERTIARY CUE TONE OPERATION	1. Check cue filter hybrid H310 at the defective cue tone output. **Cue Tone — Pin** Primary — 19 Secondary — 21 Tertiary — 11 2. Check defective cue tone detector. **Cue Tone — Detector** Primary — U12C Secondary — U12D Tertiary — U12B
NO FSK OUTPUT	1. Check cue filter hybrid H310 at pin 13. 2. Check integrated circuits U10 and U11.

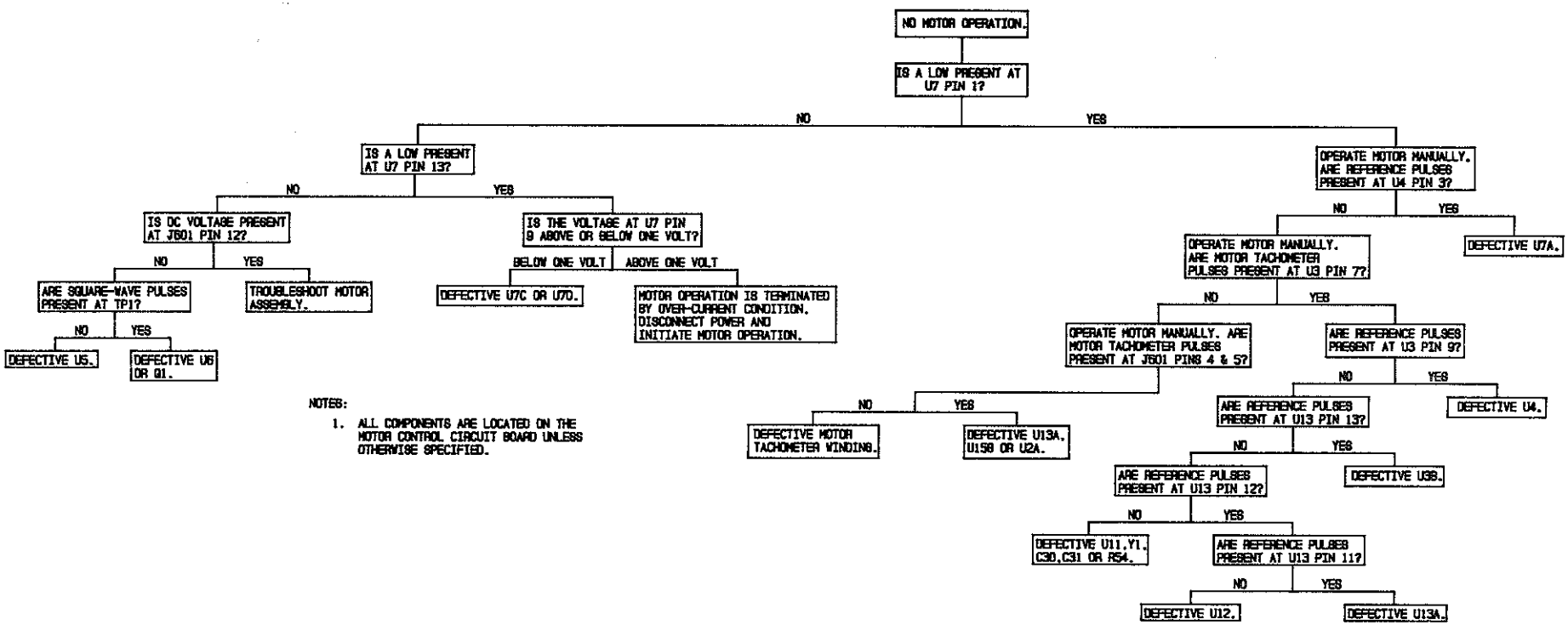


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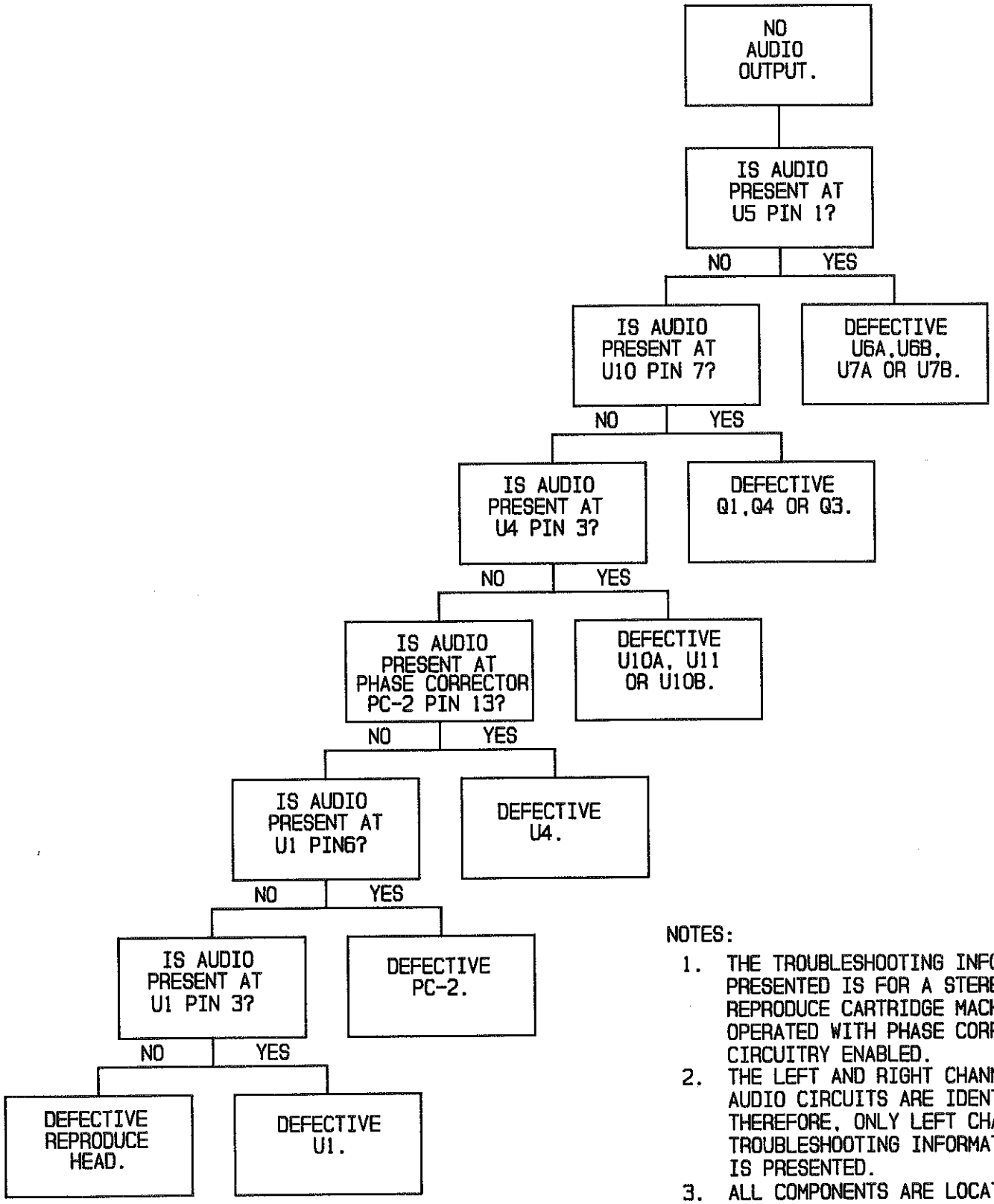
FIGURE 5-15. TROUBLESHOOTING TREE, NO MOTOR OPERATION



NOTES:

1. THE TROUBLESHOOTING INFORMATION PRESENTED IS FOR A STEREO PT-90 REPRODUCE CARTRIDGE MACHINE OPERATED WITH PHASE CORRECTION CIRCUITRY ENABLED.
2. THE LEFT AND RIGHT CHANNEL AUDIO CIRCUITS ARE IDENTICAL. THEREFORE, ONLY LEFT CHANNEL TROUBLESHOOTING INFORMATION IS PRESENTED.
3. ALL COMPONENTS ARE LOCATED ON THE AUDIO CIRCUIT BOARD UNLESS OTHERWISE SPECIFIED.

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FIGURE 5-16. TROUBLESHOOTING TREE, NO AUDIO OUTPUT

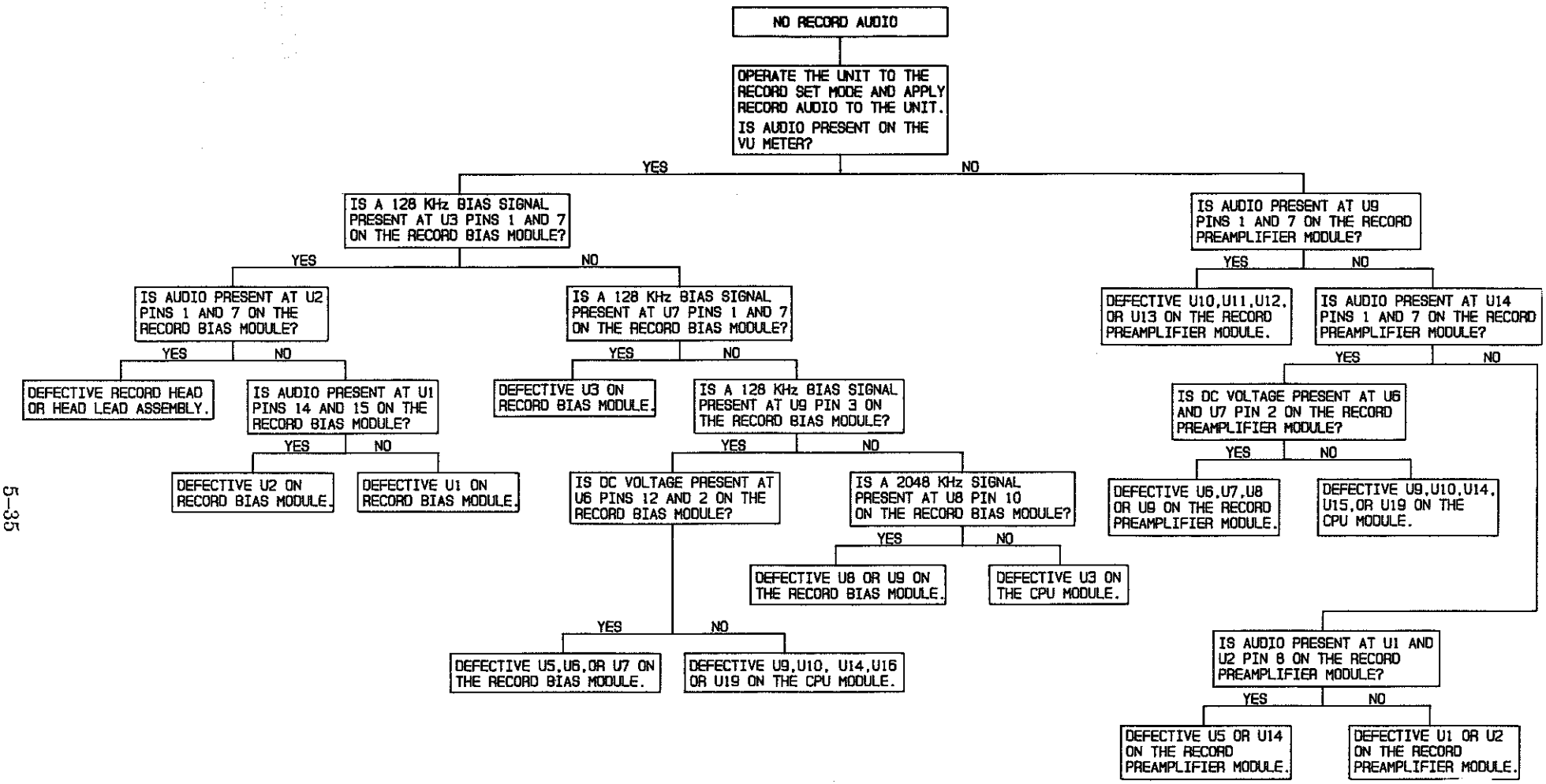

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FIGURE 5–17. TROUBLESHOOTING TREE, NO RECORD AUDIO

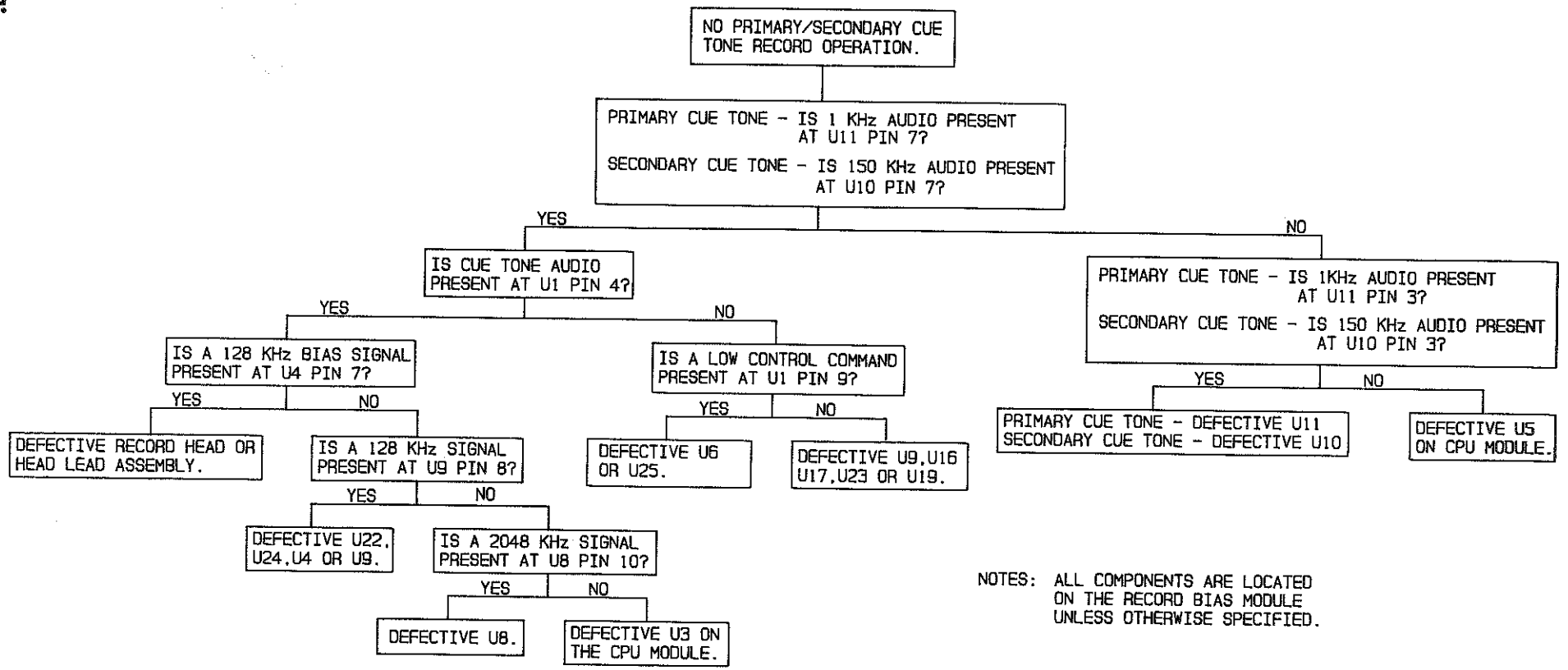

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FIGURE 5-18. TROUBLESHOOTING TREE, NO PRIMARY/SECONDARY CUE TONE RECORD OPERATION

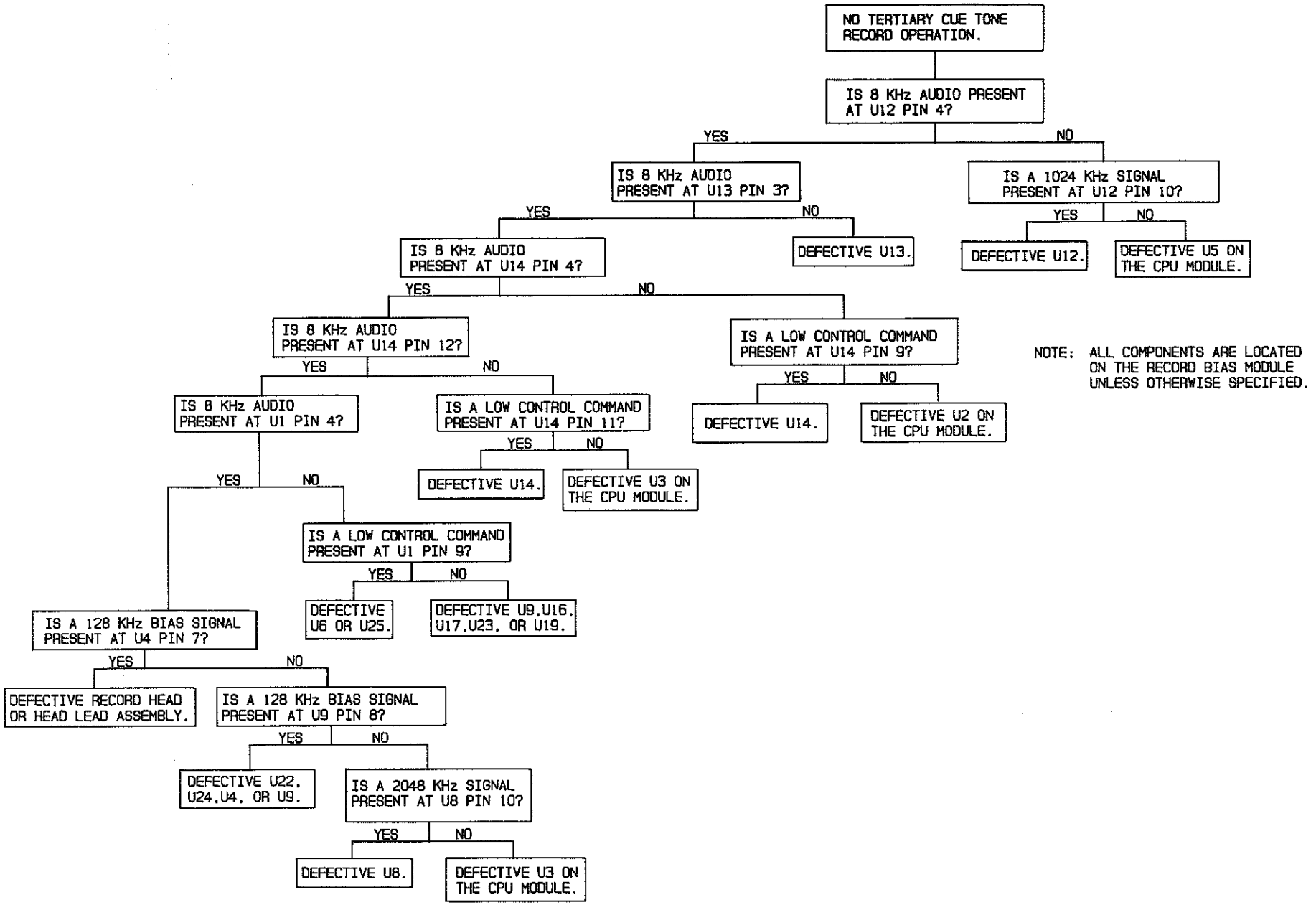

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FIGURE 5-19.
TROUBLESHOOTING TREE, NO TERITARY CUE TONE RECORD OPERATION

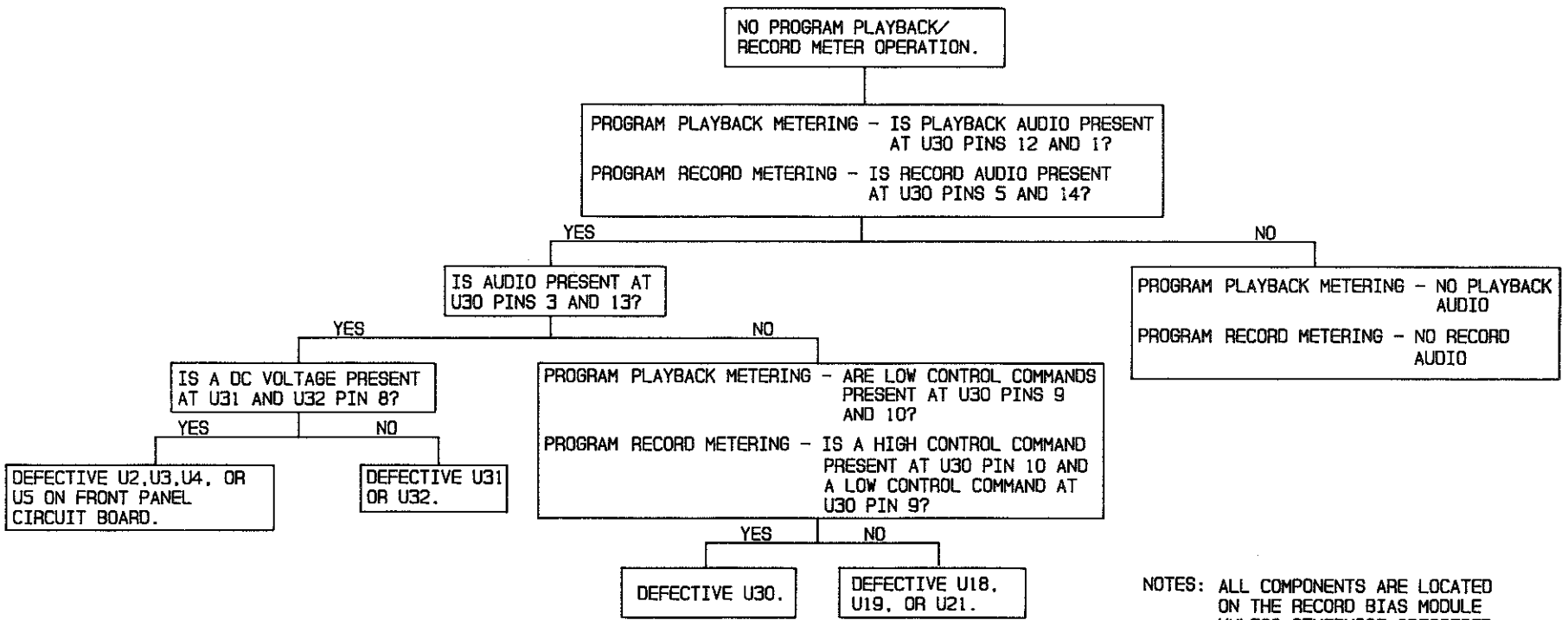

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FIGURE 5-20. TROUBLESHOOTING TREE, NO PROGRAM PLAYBACK/RECORD METER OPERATION

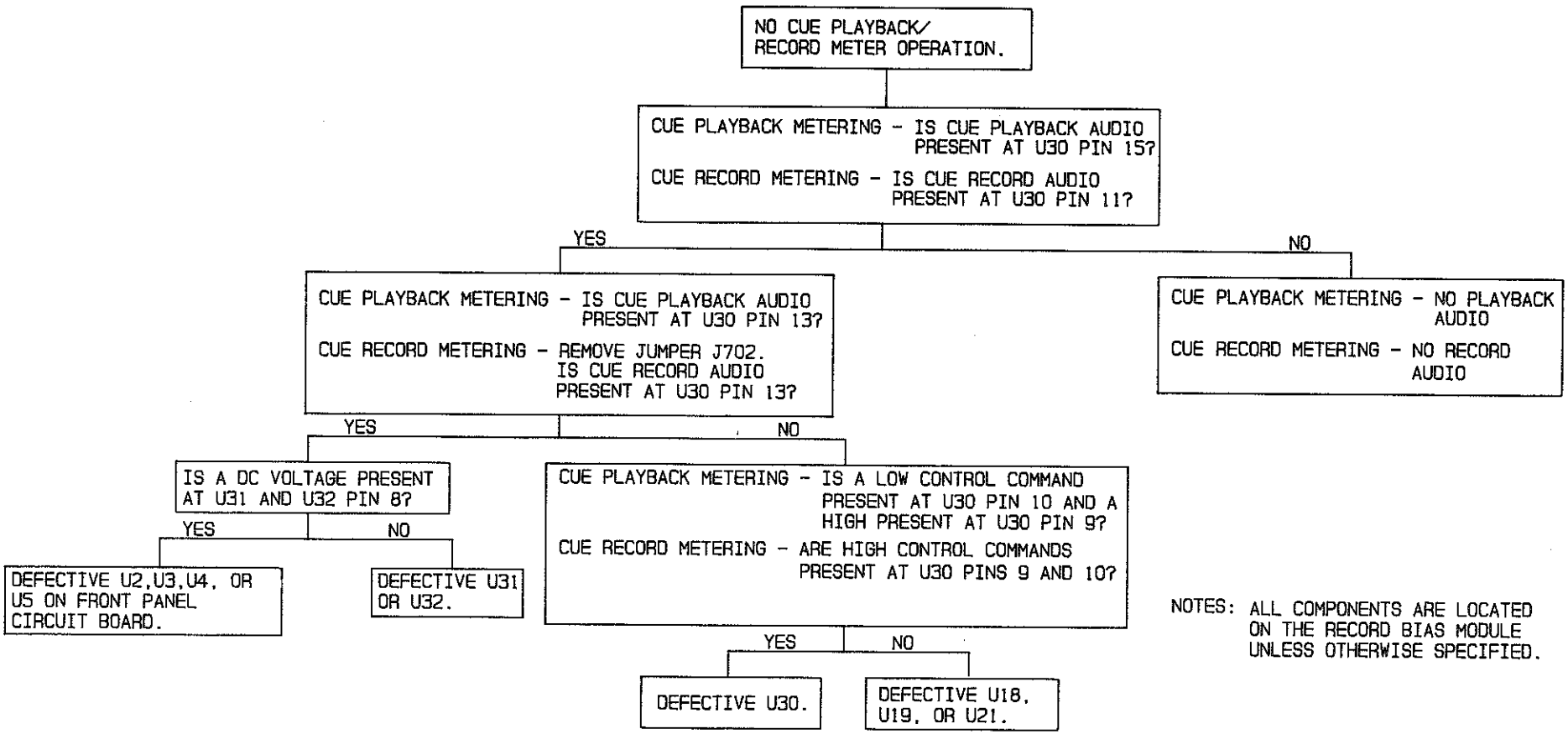

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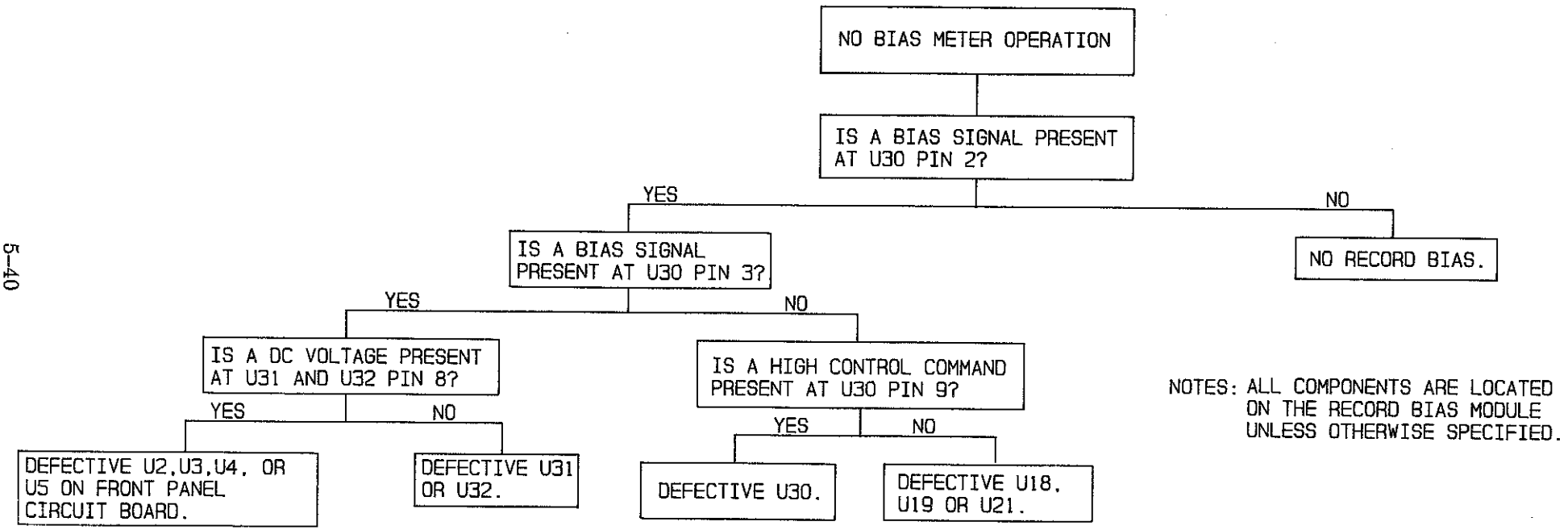
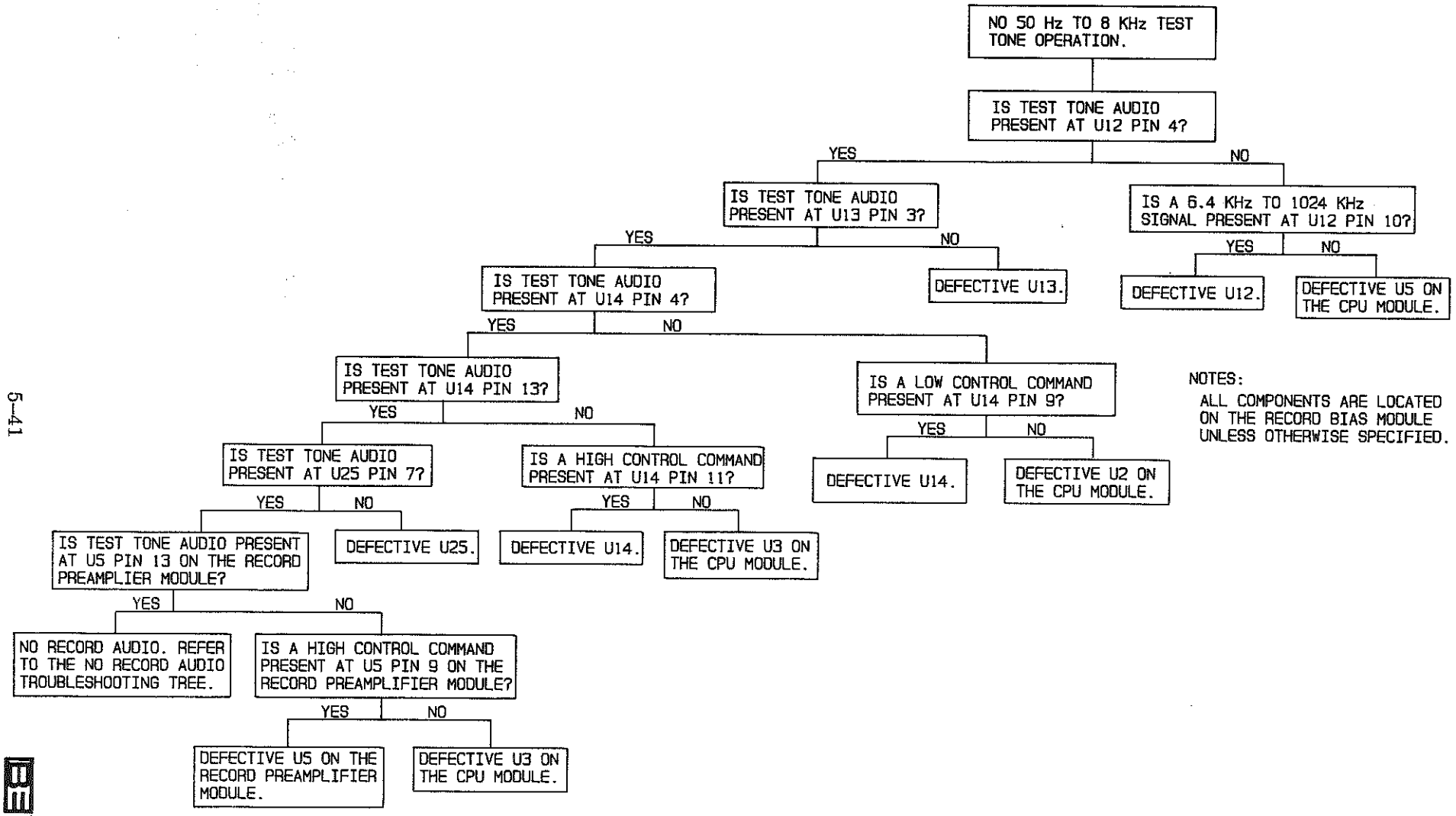
FIGURE 5-21. TROUBLESHOOTING TREE, NO CUE PLAYBACK/RECORD METER OPERATION



597–9000–72

FIGURE 5–22. TROUBLESHOOTING TREE, NO BIAS METER OPERATION



597-9000-73

FIGURE 5-23. TROUBLESHOOTING TREE, NO 50 Hz TO 8 kHz TEST TONE OPERATION

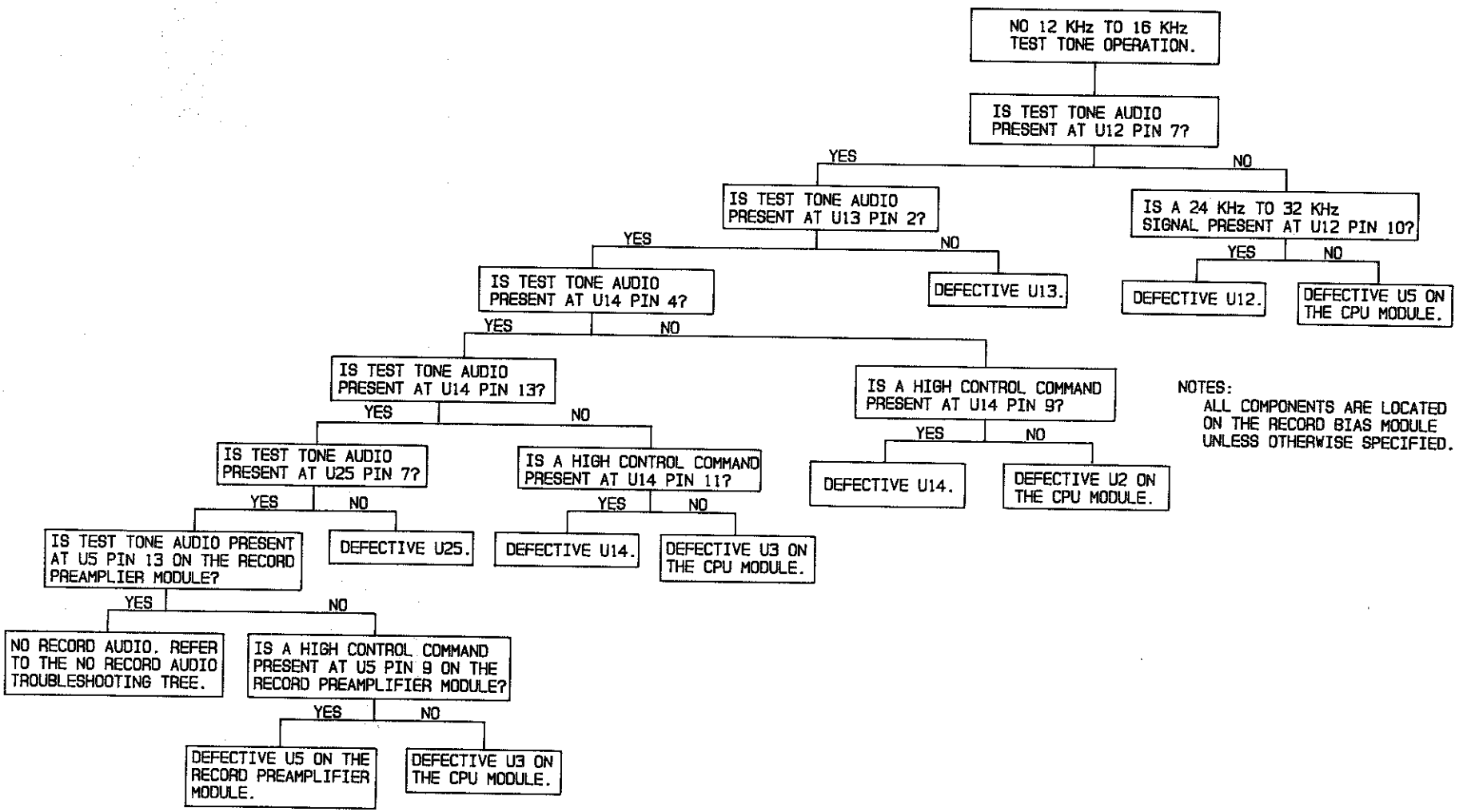


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FIGURE 5–24.
TROUBLESHOOTING TREE, NO 12 kHz TO 16 kHz TEST TONE OPERATION

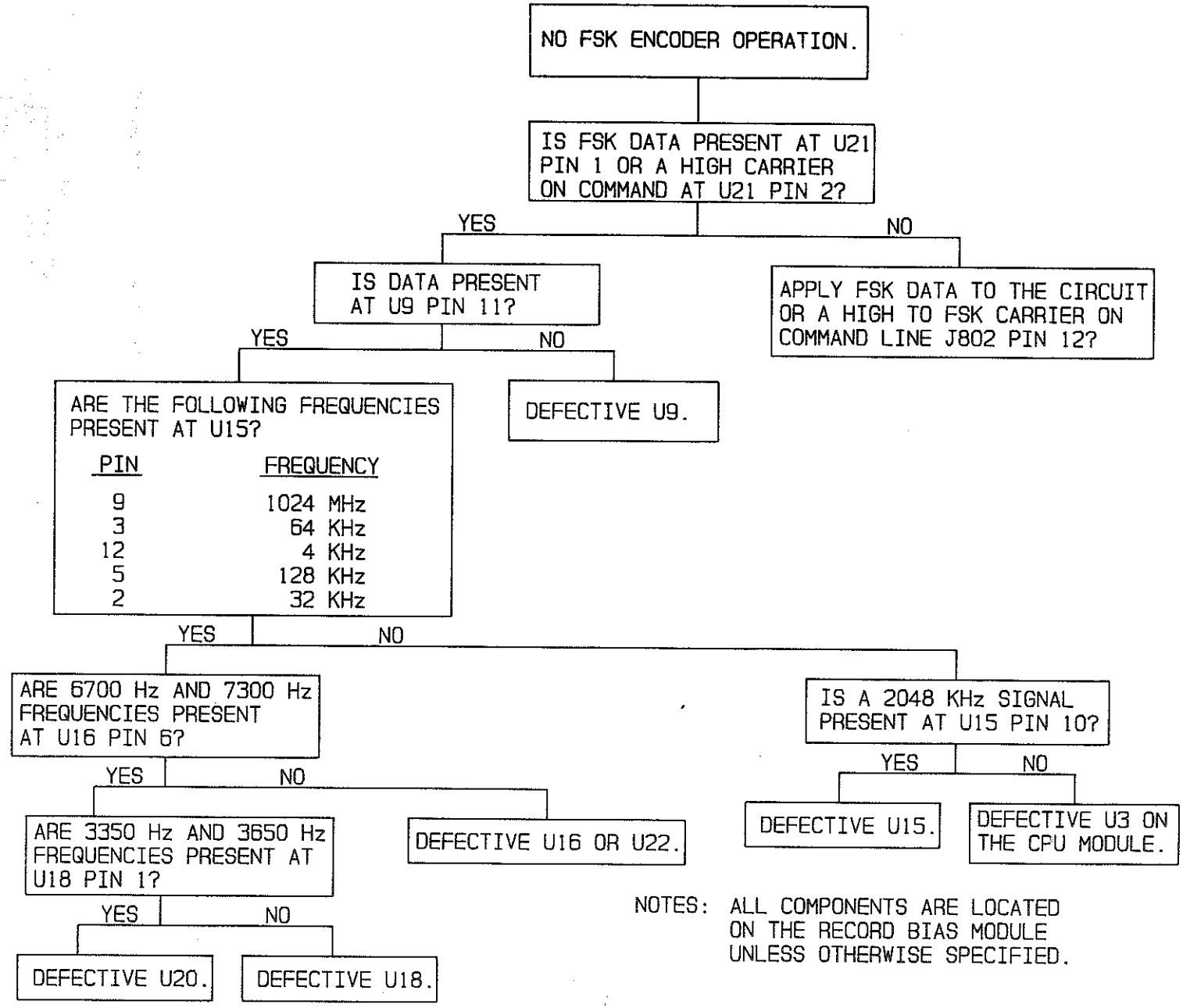

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FIGURE 5-25. TROUBLESHOOTING TREE, NO FSK ENCODER OPERATION

WARNING

WARNING

DISCONNECT ALL CARTRIDGE MACHINE PRIMARY POWER BEFORE REMOVING OR INSERTING PRINTED CIRCUIT BOARDS OR REPLACING ANY COMPONENTS.

CAUTION

CAUTION

INADVERTENT CONTACT BETWEEN ADJACENT COMPONENTS OR CIRCUIT BOARDS WITH TEST EQUIPMENT MAY CAUSE SERIOUS DAMAGE TO THE CARTRIDGE MACHINE.

5–352. Once trouble is isolated and power is totally deenergized, refer to the schematic diagrams and the theory of operation to assist in problem resolution. The defective component may be repaired locally or the entire device may be returned to Broadcast Electronics Inc. for repair or replacement.

WARNING

WARNING

DISCONNECT POWER BEFORE REMOVING OR REPLACING CIRCUIT BOARDS OR COMPONENTS.

CAUTION

CAUTION

WHEN REPLACING A COMPONENT MOUNTED ON A HEAT–SINK, ENSURE A THIN FILM OF A ZINC–BASED HEAT–SINK COMPOUND IS USED TO ASSURE GOOD HEAT DISSIPATION.

5–353. **COMPONENT REPLACEMENT.** The circuit boards used in the PT–90 cartridge machines are double–sided with plated–through holes. Due to the plated–through hole design, solder fills the holes by capillary action. This condition requires that defective components be removed carefully to avoid damage to the circuit board.

5–354. On all circuit boards, the adhesion between the copper trace and the circuit board fails at almost the same temperature as solder melts. A circuit board trace can be destroyed by excessive heat or lateral movement during soldering. Use of a small soldering iron with steady pressure is required for circuit board repairs.

5–355. To remove a soldered component from a circuit board, cut the leads from the body of the defective component while the device is still soldered to the board. Grip a component lead with needle–nose pliers. Touch the soldering iron to the lead at the solder connection on the circuit side of the board. When the solder begins to melt, push the lead through the back side of the board and cut off the clinched end of the lead. Each lead may now be heated independently and pulled out of each hole. The holes may be cleared by careful re–heating with a low wattage iron and removing the residual solder with a soldering vacuum tool.

5–356. Install the new component and apply solder from the circuit side of the board. If no damage has been incurred to the plated–through holes, soldering of the component side of the board will not be required.

WARNING

WARNING

MOST SOLVENTS WHICH REMOVE ROSIN FLUX ARE VOLATILE AND TOXIC BY NATURE AND SHOULD BE USED ONLY IN SMALL AMOUNTS IN A WELL VENTILATED AREA AWAY FROM FLAME, CIGARETTES, AND HOT SOLDERING IRONS.

WARNING

WARNING

OBSERVE THE MANUFACTURERS CAUTIONARY INSTRUCTIONS.

5–357. After soldering, remove residual flux with a suitable solvent. Rubbing alcohol is highly diluted and is not effective.

5–358. The board should be checked to ensure the flux has been completely removed. Rosin flux is not normally corrosive, however in time, the flux will absorb enough moisture to become conductive and create problems.

5–359. **INTEGRATED CIRCUITS.** Special care should be exercised with integrated circuits. Each integrated circuit must be installed by matching the integrated circuit notch with the notch on the socket. Do not attempt to remove an integrated circuit from a socket with your fingers. Use an integrated circuit puller to lightly pry the component from the socket.

SECTION VI
PARTS LISTS

6–1. INTRODUCTION.

6–2. This section provides descriptions and part numbers of electrical components, assemblies, and selected mechanical parts required for maintenance of the Broadcast Electronics PT–90 series cartridge machines. Each table entry in this section is indexed by reference designators appearing on the applicable schematic diagram.

TABLE 6–1. REPLACEABLE PARTS LIST INDEX

TABLE 6–2. PT–90 PLAYBACK FINAL ASSEMBLIES – 900–9000–000, 900–9002–000

REF. DES.	DESCRIPTION	PART NO.	QTY.
——	Head, Dummy, H801016	407–0001	1
——	Head Box Assembly	950–0302	1
——	Accessory Kit	950–0081	1
——	PT–90 Playback Basic Assembly	950–9000	1
	ADDITIONAL PARTS FOR MONOPHONIC ASSEMBLY 900–9000–000		
——	Head, Playback, Monophonic, 2–Channel, Model NPD1484 Inductance at 1 kHz: 475 mH Impedance at 1 kHz: 3.3 Ohms DC Resistance: 500 Ohms	250–0006	1
——	Monophonic Audio Module Assembly	950–0033	1
	ADDITIONAL PARTS FOR STEREOPHONIC ASSEMBLY 900–9002–000		
——	Head, Playback, Stereophonic, 3–Channel, Model NPD1496 Inductance at 1 kHz: 475 mH Impedance at 1 kHz: 3.3 Ohms DC Resistance: 500 Ohms	250–0007	1
——	Stereophonic Audio Module Assembly	950–0034	1

TABLE 6–3. PT–90 RECORD/PLAYBACK FINAL ASSEMBLIES 900–9003–000, 900–9003–300 (Sheet 1 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
	117V50/60 Hz		
F1	Fuse, AGC, 1A, 250V, Slow–Blow	334–0100	2
	220V 50/60 Hz		
F1	Fuse, AGC, 1/2A, 250V, Slow–Blow	334–0050	2
S1	Switch, Pushbutton, Rectangular, Momentary Contact, Illuminated (**START** Switch)	340–0103	1
S2,S3	Switch, Pushbutton, Square, Momentary Contact, Incandescent, Standard Bezel (**F FWD** and **STOP** Switches)	340–0104	2
S4	Switch, Pushbutton, Square, Momentary Contact, Incandescent, Guarded Bezel (**RECORD** Switch)	340–0094	1
——	Guide, Card, Nylon, 2.5 Inches (6.35 cm)	409–0020	7
——	Guide, Card, Nylon, 6 Inch (15.24 cm)	409–0002	7
——	Head, Playback, Stereophonic, 3–Channel, Model NPD1496 Inductance at 1 kHz: 475 mH Impedance at 1 kHz: 3.3 Ohms DC Resistance: 500 Ohms	250–0007	1
——	Head, Record, Stereophonic, 3–Channel, Model F38B9303 Inductance at 1 kHz: 0.10 mH Impedance at 1 kHz: 4.6 Ohms DC Resistance: 4.9 Ohms	250–0010	1
——	Switch Cap, Square, Yellow (STOP)	340–0014	1
——	Switch Cap, Square, Blue (F FWD)	340–0059	1
——	Switch Cap, Rectangular, Green (START)	340–0089	1
——	Switch Cap, Square, Red (RECORD)	343–0043	1

TABLE 6–3. PT–90 RECORD/PLAYBACK FINAL ASSEMBLIES 900–9003–000, 900–9003–300 (Sheet 2 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
——	Lamp, Wedge–base, No. 85, 28V @ 0.04 Amperes	321–0085	4
——	Blank Switch Circuit Board	510–9010	1
	117V50/60 Hz		
——	AC Line Cord, CEE 7/7 3–Wire European Plug	681–0001	1
	220V 50/60 Hz		
——	AC Line Cord, CEE 7/7 3–Wire European Plug	682–0003	1
——	PT–90 Record/Playback Deck Assembly	950–0300–005	1
——	Stereophonic Audio Module Assembly	950–0034	1
——	PT–90 Record Pre–Amplifier Module Assembly	950–0104	1
——	Power Supply Module Assembly	950–0032–001	1
——	Logic Module Assembly	950–0035	1
——	CPU Module Assembly	950–0101	1
——	Record/Bias Module Assembly	950–0102	1
——	Motherboard Assembly	910–9013	1
——	PT–90 Record/Playback Accessory Kit	950–0082	1
——	Phase–Lok V Head Box Assembly	950–0302	1
——	Front Panel Circuit Board Assembly	910–9011	1
——	Motor Control Circuit Board Assembly	910–9005	1
——	PT–90 Motor Assembly	950–0037	1
——	Record/Playback Cable Assembly	940–0032	1

TABLE 6–4. PT–90 PLAYBACK ACCESSORY KIT – 950–0081

REF. DES.	DESCRIPTION	PART NO.	QTY.
F1	Fuse, AGC, 1/2A, 250V, Slow–Blow	334–0050	1
——	AC Line Cord, N.E.M.A. 3–Wire North American Plug	682–0001	1
——	Receptacle, Female, 3–Pin, XLR Type	829–4216	2
——	Connector Plug, 25–Pin	417–0251	1
——	Pins	418–0048	25
——	Kit, Cable Clamp Assembly (with spring latch), 25–Pin	418–2501	1
——	Label, Elevated Level (For Cartridges)	594–0093	25
——	Pressure Roller Indentation Gauge	300–0013	1

TABLE 6–5. PT–90 RECORD/PLAYBACK ACCESSORY KIT – 950–0082

REF. DES.	DESCRIPTION	PART NO.	QTY.
F1	Fuse, 3AG, 1A, 250V, Slow–Blow	334–0100	1
——	AC Line Cord, N.E.M.A. 3–Wire North American Plug	682–0001	1
——	Receptacle, Female, 3–Pin, XLR Type	829–4216	2
——	Plug, Male, 3–Pin, XLR Type	829–4217	2
——	Connector Plug, 25–Pin	417–0251	1
——	Receptacle, 25–Pin	417–0252	1
——	Pins	418–0048	25
——	Socket Pins	417–0158	25
——	Label, Elevated Level (For Cartridges)	594–0093	25
——	Pressure Roller Indentation Gauge	300–0013	1

TABLE 6–6. PT–90 PLAYBACK BASIC ASSEMBLY – 950–9000

REF. DES.	DESCRIPTION	PART NO.	QTY.
S1	Switch, Pushbutton, Rectangular, Momentary Contact, Illuminated (**START** Switch)	340–0103	1
S2,S3	Switch, Pushbutton, Square, Momentary Contact, Incandescent (**F FWD** and **STOP** Switches)	340–0104	2
——	Switch Cap, Yellow, Square (**STOP**)	340–0014	1
——	Switch Cap, Blue, Square (**F FWD**)	340–0059	1
——	Switch Cap, Green, Rectangular (**START**)	340–0089	1
——	Lamp, Wedge Base, No. 85, 28V @ 0.04 Amperes	321–0085	3
——	Cartridge Guide, Left	445–0008	1
——	Spring, Cartridge Guide, Left	430–0010	1
——	Pressure Pad, Cartridge Guide	459–0123	1
——	Spring, Pressure Pad	430–0011	2
——	Guide, Circuit Board 2 1/2 Inch	409–0020	4
——	Guide, Circuit Board	409–0002	4
——	Blank Circuit Board, Front Panel Switch	510–9002	1
——	Deck Assembly	950–0300–004	1
——	Power Supply Module Assembly	950–0032–001	1
——	Logic Module Assembly	950–0035	1
——	Motherboard Assembly	910–9006	1
——	Front Panel Status Circuit Board Assembly	910–9003–1	1
——	Motor Control Circuit Board Assembly	910–9005	1
——	PT–90 Motor Assembly	950–0037	1
——	Playback Cable Assembly	940–0030	1

TABLE 6–7. PT–90 HEAD BOX ASSEMBLY – 950–0302

REF. DES.	DESCRIPTION	PART NO.	QTY.
——	Tape Guide	445–0004	2
——	Spring, Head Box	430–0012	6

TABLE 6–8. PLAYBACK DECK ASSEMBLY – 950–0300–004

REF. DES.	DESCRIPTION	PART NO.	QTY.
S4	Switch, Micro, Roller Actuator, SPDT, 5 Amperes @ 125V ac (Deck Ready Switch)	346–0027	1
——	Pressure Roller	444–0700	1
——	Pressure Roller Shaft	446–0056	1
——	Pressure Roller Cross Shaft	446–0059	1
——	Retainer, "E" Ring	454–3318	1
——	Washer, Nylon (for Pressure Roller) Outside Diameter: 0.312 Inches (0.792 cm) Inside Diameter: 0.190 Inches (0.483 cm) Height: 0.010 Inches (0.254 cm)	423–5008	1
——	Washer, Nylon (for Pressure Roller) Outside Diameter: 0.312 Inches (0.792 cm) Inside Diameter: 0.190 Inches (0.483 cm) Height: 0.015 Inches (0.381 cm)	423–5009	1
——	Cartridge Guide, Right	445–0006	1
——	Pressure Pad, Cartridge Guide	459–0123	1
——	Pressure Pad Spring	430–0011	2
——	Solenoid Stop	459–0125	1
——	Spring, Solenoid Return	430–0014	1
——	Solenoid Assembly	950–0303–001	1
——	Reflective Sensor Assembly	950–0306	1

TABLE 6–9. RECORD/PLAYBACK DECK ASSEMBLY – 950–0300–005

REF. DES.	DESCRIPTION	PART NO.	QTY.
S4	Switch, Micro, Roller Actuator, SPDT, 5 Amperes @ 125V ac (Deck Ready Switch)	346–0027	1
——	Pressure Roller	444–0700	1
——	Pressure Roller Shaft	446–0056	1
——	Pressure Roller Cross Shaft	446–0059	1
——	Retainer "E" Ring	454–3318	1
——	Cartridge Guide, Left	445–0007	1
——	Cartridge Guide, Right	445–0006	1
——	Pressure Pad, Cartridge Guide	459–0123	2
——	Spring, Pressure Pad	430–0011	4
——	Spring, Cartridge Guide, Left	430–0010	1
——	Solenoid Stop	459–0125	1
——	Spring, Solenoid Return	430–0014	1
——	Washer, Nylon (for Pressure Roller) Outside Diameter: 0.312 Inches (0.792 cm) Inside Diameter: 0.190 Inches (0.483 cm) Height: 0.010 Inches (0.254 cm)	423–5008	1
——	Washer, Nylon (for Pressure Roller) Outside Diameter: 0.312 Inches (0.792 cm) Inside Diameter: 0.190 Inches (0.483 cm) Height: 0.015 Inches (0.381 cm)	423–5009	1
——	Solenoid Assembly	950–0303–001	1
——	Reflective Sensor Assembly	950–0306	1

TABLE 6–10. SOLENOID ASSEMBLY – 950–0303–001

REF. DES.	DESCRIPTION	PART NO.	QTY.
L1	Solenoid, 32V dc, 1.75 Diameter, Resistance: 37.5 Ohms ±10% at 255C	280–0003	1
——	Pins, Crimp Type	417–8766	2

TABLE 6–11. REFLECTIVE SENSOR – 950–0306

REF. DES.	DESCRIPTION	PART NO.	QTY.
LP1	Reflective Assembly, HOA–1180–1	320–0019	1
——	Connector Housing, 5–Pin In–line	417–0165	1
——	Pins, Crimp Type	417–8766	4
——	Keying Plug	417–0144	1

TABLE 6–12. MONOPHONIC/STEREOPHONIC PLAYBACK AUDIO MODULE ASSEMBLIES – 950–0033, 950–0034 (Sheet 1 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C3	Capacitor, Mica, 68 pF ±5%, 500V	040–6813	1
C5	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C6	Capacitor, Mica, 10 pF ±5%, 500V	042–1012	1
C7	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C8	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030–1033	1
C9	Capacitor, Electrolytic, 4.7 uF, 35V	024–4764	1
C10	Capacitor, Electrolytic, 47 uF, 16V	013–4750	1
C17	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C19,C20	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C21	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C25 THRU C27,C29	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	4
C30,C31	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	2
C32,C37	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C38	Capacitor, Mica, 22 pF, 500V	040–2213	1
C39,C40	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C45	Capacitor, Electrolytic, 47 uF, 16V	013–4750	1
C47	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	1
C49	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C51	Capacitor, Mica, 1000 pF ±1%, 100V	041–1031	1
C52	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C53	Capacitor, Mylar Film, 0.047 uF ±10%, 100V	030–4743	1
C54	Capacitor, Monolythic Ceramic, 0.0047 uF ±5%, 100V	003–4723	1
C55	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	1
C56	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C57,C58	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C59,C60	Capacitor, Electrolytic, 4.7 uF, 35V	024–4764	2
C61	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C62	Capacitor, Electrolytic, 33 uF, 35V	024–3335	1

TABLE 6–12. MONOPHONIC/STEREOPHONIC PLAYBACK AUDIO MODULE ASSEMBLIES – 950–0033, 950–0034 (Sheet 2 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C63,C64	Capacitor, Electrolytic, 4.7 uF, 35V	024–4764	2
C67	Capacitor, Electrolytic, 47 uF, 16V	013–4750	1
C68,C69	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C70	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C81	Capacitor, Ceramic Disc, 10 pF ±10%, 1000V	001–1014	1
C85	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C88,C89	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C90	Capacitor, Mylar Film, 0.022 uF ±10%, 200V	031–2243	1
C92	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C93,C94	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
D1	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	1
J402	Connector, Header, 3–Pin	417–0003	1
J405	Connector, Audio, XLB Series, 3–Pin	418–0049	1
J407,J408	Connector, Header, 3–Pin	417–0003	2
J412	Jack, Phone	417–0150	1
P401	Receptacle, 50–Pin Dual In–line	417–0147	1
P402,P407	Jumper Switch, Programmable, 2–Pin	340–0004	2
Q1	Field Effect Transistor, J271, P–Channel JFET, TO–92 Case	210–0271	1
Q3	Transistor, 2N3904, NPN, Silicon, TO–92 Case	211–3904	1
Q4	Field Effect Transistor, J271, P–Channel JFET, TO–92 Case	210–0271	1
R1	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R3	Resistor, 270 k Ohm ±5%, 1/4W	100–2763	1
R5	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R7	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R8	Resistor, 68 k Ohm ±5%, 1/4W	100–6853	1
R9	Resistor, 680 Ohm ±5%, 1/4W	100–6833	1
R10	Resistor, 1.2 k Ohm ±5%, 1/4W	100–1243	1
R11	Potentiometer, 10 k Ohm ±10%, 1/2W	178–1054	1
R19	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R20	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R21	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R22	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R23	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R24	Resistor, 110 k Ohm ±5%, 1/4W	100–1163	1
R25	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R26	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R27	Resistor, 56 k Ohm ±5%, 1/4W	100–5653	1
R32	Resistor, 4.53 k Ohm ±1%, 1/4W	103–4534	1
R38	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R40	Potentiometer, 500 k Ohm ±10%, 1 1/2W	178–5065	1
R41	Resistor, 2.2 k Ohm ±5%, 1/4W	100–2243	1
R42	Resistor, 47 k Ohm ±5%, 1/4W	100–4753	1
R47	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R48	Resistor, 4.7 k Ohm ±5%, 1/4W	100–4743	1
R49,R53, R54,R57, R58	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	5
R61,R62	Resistor, 15 Ohm ±5%, 1/4W	100–1523	2
R63	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1

TABLE 6–12. MONOPHONIC/STEREOPHONIC PLAYBACK AUDIO MODULE ASSEMBLIES – 950–0033, 950–0034 (Sheet 3 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R64	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R65,R66	Resistor, 15 Ohm ±5%, 1/4W	100–1523	2
R73,R74	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	2
R80,R81	Resistor, 1.8 Meg Ohm ±5%, 1/4W	100–1873	2
R82	Resistor, 46.4 k Ohm ±1%, 1/4W	103–4645	1
R83	Resistor, 34.8 k Ohm ±1%, 1/4W	103–3485	1
R84	Resistor, 221 k Ohm ±1%, 1/4W	103–2216	1
R85	Resistor, 15.4 k Ohm ±1%, 1/4W	103–1551	1
R86	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	1
R87	Resistor, 15.4 k Ohm ±1%, 1/4W	103–1551	1
R88	Resistor, 150 k Ohm ±1%, 1/4W	103–1561	1
R89	Resistor, 4.75 k Ohm ±1%, 1/4W	103–4741	1
R90	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	1
R91,R92	Resistor, 1.5 Meg Ohm ±5%, 1/4W	100–1573	2
R93	Resistor, 46.4 k Ohm ±1%, 1/4W	103–4645	1
R94,R95	Resistor, 1.5 k Ohm ±1%, 1/4W	103–1504	2
R96,R97	Resistor, 124 Ohm ±1%, 1/4W	103–1241	2
R100,R101	Resistor, 665 Ohm ±1%, 1/4W	103–6653	2
R102,R103	Resistor, 124 Ohm ±1%, 1/4W	103–1241	2
R104	Resistor, 71.5 k Ohm ±1%, 1/4W	103–7155	1
R105	Resistor, 46.4 k Ohm ±1%, 1/4W	103–4645	1
R110	Resistor, 4.7 k Ohm ±5%, 1/4W	100–4743	1
R112 THRU R115	Resistor, 10 Ohm ±5%, 1/4W	100–1023	4
R126	Resistor, 47.5 k Ohm ±1%, 1/4W	103–4755	1
R127	Resistor, 3.01 k Ohm ±1%, 1/4W	103–3014	1
R132	Resistor, 47 k Ohm ±5%, 1/4W	100–4753	1
R135,R136	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R137,R138	Resistor, 68 Ohm ±5%, 1/2W	110–6823	2
U1	Integrated Circuit, NE5534AN, Low Noise Operational Amplifier, 8–Pin DIP	221–5534	1
U3	Integrated Circuit, TLO72CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U4	Integrated Circuit, MC14052B, Dual 4–Channel Analog Multiplexers/Demultiplexers, CMOS MSI, 2P4T, 16–Pin DIP	220–4052	1
U5	Integrated Circuit, TLO72CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U6,U7	Integrated Circuit, NE5532AP, Dual Low Noise Operational Amplifier, 8–Pin DIP	221–5532–001	2
U10	Integrated Circuit, TLO74CN, Quad JFET–Input Operational Amplifier, 14–Pin DIP	221–0074	1
U11	Integrated Circuit, CRL2200, Single–Channel Noise Reduction System, 16–Pin DIP	220–2200	1
U13	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
U14	Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0337	1
U15	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
U16	Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0337	1

TABLE 6-12. MONOPHONIC/STEREOPHONIC PLAYBACK AUDIO MODULE ASSEMBLIES - 950-0033, 950-0034 (Sheet 4 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
XU1,XU3	Socket, 8-Pin DIP	417-0804	2
XU4	Socket, 16-Pin DIP	417-1604	1
XU5 THRU XU7	Socket, 8-Pin DIP	417-0804	3
XU10	Socket, 14-Pin DIP	417-1404	1
XU11	Socket, 16-Pin DIP	417-1604	1
——	Pins, Crimp Type	417-8766	3
——	Blank Circuit Board, Audio	510-9000	1
	ADDITIONAL PARTS FOR MONOPHONIC ASSEMBLY 950-0033		
R6	Potentiometer, 250 k Ohm 10%, 1/2W	180-0001	1
J407	Connector Housing, 3-Pin	417-0003-001	1
	ADDITIONAL PARTS FOR STEREOPHONIC ASSEMBLY 950-0034		
C2	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C4	Capacitor, Mica, 68 pF ±5%, 500V	040-6813	1
C11	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C12	Capacitor, Mica, 10 pF ±5%, 500V	042-1012	1
C13	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C14	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030-1033	1
C15	Capacitor, Electrolytic, 4.7 uF, 35V	024-4764	1
C16	Capacitor, Electrolytic, 47 uF, 16V	013-4750	1
C18	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C22	Capacitor, Electrolytic, 10 uF, 25V	023-1075	1
C23,C24	Capacitor, Electrolytic, 10 uF, 35V	023-1076	2
C28,C33	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C34,C35	Capacitor, Mica, 100 pF, 500V	040-1022	2
C36,C41	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C42	Capacitor, Mica, 22 pF, 500V	040-2213	1
C43,C44	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C46	Capacitor, Electrolytic, 47 uF, 16V	013-4750	1
C48	Capacitor, Mica, 100 pF, 500V	040-1022	1
C50	Capacitor, Mylar Film, 0.01 uF, 100V	031-1043	1
C65	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C71 THRU C74	Capacitor, Electrolytic, 47 uF, 16V	013-4750	4
C75	Capacitor, Mica, 1000 pF ±1%, 100V	041-1031	1
C76	Capacitor, Electrolytic, 1 uF, 50V	024-1064	1
C77	Capacitor, Mylar Film, 0.047 uF, 100V	030-4743	1
C78	Capacitor, Monolythic Ceramic, 0.0047 uF ±5%, 100V	003-4723	1
C79	Capacitor, Mica, 100 pF, 500V	040-1022	1
C80	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C82	Capacitor, Ceramic Disc, 10 pF ±10%, 1000V	001-1014	1
C83	Capacitor, Electrolytic, 47 uF, 16V	013-4750	1
C84	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C86	Capacitor, Electrolytic, 1 uF, 50V	024-1064	1
C87	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C91	Capacitor, Mylar Film, 0.022 uF, 200V	031-2243	1

TABLE 6-12. MONOPHONIC/STEREOPHONIC PLAYBACK AUDIO MODULE ASSEMBLIES - 950-0033, 950-0034 (Sheet 5 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
	ADDITIONAL PARTS FOR STEREOPHONIC ASSEMBLY 950-0034 (Cont'd)		
J403	Connector Header, 3-Pin	417-0003	1
J406	Connector, Audio, XLB Series, 3-Pin	418-0049	1
P403	Connector Housing, 3-Pin	417-0003-001	1
P408	Jumper Switch, Programmable	340-0004	1
PC1	Phase Detector	220-9000	1
PC2,PC3	Phase Corrector	220-9001	2
Q2,Q5	Field Effect Transistor, J271, P-Channel JFET, TO-92 Case	210-0271	2
R2	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R4	Resistor, 270 k Ohm ±5%, 1/4W	100-2763	1
R6	Potentiometer, 250 k Ohm ±10%, 1/2W	180-0001	1
R12	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
R13	Potentiometer, 250 k Ohm ±10%, 1/2W	180-0001	1
R14	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
R15	Resistor, 68 k Ohm ±5%, 1/4W	100-6853	1
R16	Resistor, 680 Ohm ±5%, 1/4W	100-6833	1
R17	Resistor, 1.2 k Ohm ±5%, 1/4W	100-1243	1
R18	Potentiometer, 10 k Ohm ±10%, 1/2W	178-1054	1
R28	Resistor, 27 k Ohm ±5%, 1/4W	100-2753	1
R29	Potentiometer, 10 k Ohm ±10%, 1/2W	177-1054	1
R30,R31	Resistor, 22 k Ohm ±5%, 1/4W	100-2253	2
R33	Resistor, 4.53 k Ohm ±1%, 1/4W	103-4534	1
R34	Resistor, 20 k Ohm ±5%, 1/4W	100-2053	1
R35	Potentiometer, 20 k Ohm ±10%, 1/2W	178-2054	1
R36,R37	Resistor, 4.53 k Ohm ±1%, 1/4W	103-4534	2
R39	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
R43	Potentiometer, 500 k Ohm ±10%, 1 1/4W	178-5065	1
R44	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	1
R45	Resistor, 47 k Ohm ±5%, 1/4W	100-4753	1
R46	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R50	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R51	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R52,R55, R56,R59,R60	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	5
R67,R68	Resistor, 15 Ohm ±5%, 1/4W	100-1523	2
R69	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R70	Resistor, 5.1 k Ohm ±5%, 1/4W	100-5143	1
R71,R72	Resistor, 15 Ohm ±5%, 1/4W	100-1523	2
R75,R76	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	2
R77	Potentiometer, 10 k Ohm ±10%, 1/2W	177-1054	1
R78	Resistor, 2.2 Meg Ohm ±5%, 1/4W	100-2273	1
R79	Resistor, 2.0 Meg Ohm ±5%, 1/4W	100-2073	1
R106 THRU R109	Resistor, 10 Ohm ±5%, 1/4W	100-1023	4
R111	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R116	Resistor, 46.4 k Ohm ±1%, 1/4W	103-4645	1

TABLE 6–12. MONOPHONIC/STEREOPHONIC PLAYBACK AUDIO MODULE ASSEMBLIES – 950–0033, 950–0034 (Sheet 6 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
	ADDITIONAL PARTS FOR STEREOPHONIC ASSEMBLY 950–0034 (Cont'd)		
R117	Resistor, 34.8 k Ohm ±1%, 1/4W	103–3485	1
R118	Resistor, 221 k Ohm ±1%, 1/4W	103–2216	1
R119	Resistor, 15.4 k Ohm ±1%, 1/4W	103–1551	1
R120	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	1
R121	Resistor, 15.4 k Ohm ±1%, 1/4W	103–1551	1
R122	Resistor, 1.5 Meg Ohm ±5%, 1/4W	100–1573	1
R123	Resistor, 150 k Ohm ±1%, 1/4W	103–1561	1
R124	Resistor, 4.75 k Ohm ±1%, 1/4W	103–4741	1
R125	Resistor, 1.5 Meg Ohm ±5%, 1/4W	100–1573	1
R128	Resistor, 46.4 k Ohm ±1%, 1/4W	103–4645	1
R129	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	1
R130	Resistor, 71.5 k Ohm ±1%, 1/4W	103–7155	1
R131	Resistor, 46.4 k Ohm ±1%, 1/4W	103–4645	1
R133,R134	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	2
R139	Resistor, 27 k Ohm ±5%, 1/4W	100–2753	1
R140	Potentiometer, 10 k Ohm ±10%, 1/2W	177–1054	1
R141,R142	Resistor, 22 k Ohm ±5%, 1/4W	100–2253	2
U2	Integrated Circuit, NE5534AN, Low Noise Operational Amplifier, 8–Pin DIP	221–5534	1
U8,U9	Integrated Circuit, NE5532AP, Dual Low Noise Operational Amplifier, 8–Pin DIP	221–5532–001	2
U12	Integrated Circuit, CRL2200, Single–Channel Noise Reduction System, 16–Pin DIP	220–2200	1
XU2,XU8, XU9	Socket, 8–Pin DIP	417–0804	3
XU12	Socket, 16–Pin DIP	417–1604	1

TABLE 6–13. LOGIC MODULE ASSEMBLY – 950–0035 (Sheet 1 of 5)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C2	Capacitor, Mica, 220 pF ±5%, 500V	040–2223	1
C3	Capacitor, Electrolytic, 100 uF, 25V	023–1084	1
C4	Capacitor, Mylar Film, 0.01 uF ±10%, 100V	031–1043	1
C5,C6	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C8	Capacitor, Ceramic Disc, 10 pF ±10%, 1 kV, Non–Polarized	001–1014	1
C9,C10	Capacitor, Monolythic Ceramic, 0.01 uF ±5%, 100V	003–1013	2
C11	Capacitor, Mylar Film, 0.022 uF ±10%, 200V	031–2243	1
C12,C19,C20	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	3
C21,C22	Capacitor, Electrolytic, 4.7 uF, 35V	024–4753	2
C23,C24	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C35,C37	Capacitor, Electrolytic, 1 uF, 50V	024–1064	2
C39	Capacitor, Electrolytic, 4.7 uF, 35V	024–4753	1

TABLE 6–13. LOGIC MODULE ASSEMBLY – 950–0035
(Sheet 2 of 5)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C40	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C41	Capacitor, Mylar Film, 0.022 uF ±10%, 200V	031–2243	1
C42	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030–1033	1
C43	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C44	Capacitor, Mylar Film, 0.047 uF ±10%, 100V	030–4743	1
C45,C46,C47	Capacitor, Mylar Film, 0.022 uF ±10%, 200V	031–2243	3
C48 THRU C51	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	4
C52,C53	Capacitor, Electrolytic, 100 uF, 25V	023–1084	2
C54	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C55	Capacitor, Electrolytic, 4.7 uF, 35V	024–4753	1
C56,C57	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C58	Capacitor, Monolythic Ceramic, 0.01 uF ±5%, 100V	003–1013	1
C59 THRU C67	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	9
C68	Capacitor, Electrolytic, 4.7 uF, 35V	024–4753	1
C69,C70	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C71	Capacitor, Electrolytic, 4.7 uF, 35V	024–4753	1
C72	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C73,C74	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C75	Capacitor, Ceramic Disc, 10 pF ±10%, 1 kV, Non–Polarized	001–1014	1
C76,C77	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C78,C79	Capacitor, Mylar Film, 0.01 uF ±10%, 100V	031–1043	2
C80	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C81,C82,C83	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	3
D1,D2,D3	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	3
D4 THRU D7	Diode, HP5082–2800, High Voltage, Schottky Barrier Type, 70V, 15 mA	201–2800	4
D8 THRU D24,	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	17
D25	Diode, 1N34, Germanium, 8.5 mA, 10V	202–0034	1
D26,D27,D28	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	3
D29	Diode, 1N34, Germanium, 8.5 mA, 10V	202–0034	1
D31,D32, D33, D35 THRU D40, D42 THRU D45	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	13
D46,D47,D48	Diode, HP5082–2800, High Voltage, Schottky Barrier Type, 70V, 15 mA	201–2800	3
D49	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	1
DS1 THRU DS3	Indicator, LED, Red, 5300E1, 2.3V @ 50 mA Maximum	320–0011	3
H310	Cue Filter Circuit, Hybrid	220–0001	1
J303	Connector Header, 4–Pin In–Line	417–0070	1
J304	Connector Header, 2–Pin In–Line	417–4004	1
J305,J306	Connector Header, 3–Pin In–Line	417–0003	2
J307	Connector Header, 2–Pin In–Line	417–4004	1
J308	Connector, 25–Pin D–Type	418–2500	1
J309	Connector Header, 2–Pin In–Line	417–4004	1
J310	Socket, 21–Pin DIP	417–0149	1
J311 THRU J313	Socket, 2–Pin DIP	417–0151	3

TABLE 6–13. LOGIC MODULE ASSEMBLY – 950–0035
(Sheet 3 of 5)

REF. DES.	DESCRIPTION	PART NO.	QTY.
J314	Connector Header, 3–Pin In–Line	417–0003	1
K1,K2	Relay, Coil: 12V dc, 800 Ohms Contacts: 100V dc @ 0.5 Amperes Maximum	270–0056	2
P301	Connector, 50–Pin Dual In–line	417–0147	1
P302 THRU P307,P309, P314	Jumper Switch, Programmable, 2–Pin	340–0004	8
Q1,Q2	Transistor, MPS–A14, Silicon, NPN, Darlington, TO–92 Case	211–0014	2
R1	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R2	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R3	Resistor, 510 Ohm ±5%, 1/4W	100–5133	1
R4	Resistor, 300 k Ohm ±5%, 1/4W	100–3063	1
R5,R6	Resistor, 10 Ohm ±5%, 1/4W	100–1023	2
R7	Resistor, 4.3 k Ohm ±5%, 1/4W	100–4343	1
R8	Resistor, 2 k Ohm ±5%, 1/4W	100–2043	1
R9	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R10	Potentiometer, 10 k Ohm ±10%, 1/2W	178–1054	1
R11	Resistor, 2 k Ohm ±5%, 1/4W	100–2043	1
R12	Resistor, 30 k Ohm ±5%, 1/4W	100–3053	1
R13	Resistor, 3 k Ohm ±5%, 1/4W	100–3043	1
R14	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R15	Resistor, 15 k Ohm ±5%, 1/4W	100–1553	1
R16	Resistor, 30 k Ohm ±5%, 1/4W	100–3053	1
R19	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R20	Resistor, 118 Ohm ±1%, 1/4W	100–1111	1
R21,R22	Resistor, 1.02 k Ohm ±1%, 1/4W	103–1024	2
R23	Resistor, 118 Ohm ±1%, 1/4W	100–1111	1
R43	Resistor, 390 k Ohm ±5%, 1/4W	100–3963	1
R44	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1
R45	Potentiometer, 5 k Ohm ±10%, 1/2W	178–5044	1
R46	Resistor, 1.8 k Ohm ±5%, 1/4W	100–1843	1
R47	Resistor, 3.9 k Ohm ±5%, 1/4W	100–3943	1
R48,R49	Resistor, 10 Ohm ±5%, 1/4W	100–1023	2
R50,R51,R52	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	3
R53	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R55	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R56	Resistor, 30 k Ohm ±5%, 1/4W	100–3053	1
R57	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1
R59	Resistor, 2 k Ohm ±5%, 1/4W	100–2043	1
R60	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1
R61	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R62	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R63	Resistor, 200 Ohm ±5%, 1/4W	100–2033	1
R67	Resistor, 3 k Ohm ±5%, 1/4W	100–3043	1
R68	Resistor, 27 k Ohm ±5%, 1/4W	100–2753	1
R69	Resistor, 390 k Ohm ±5%, 1/4W	100–3963	1
R70	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1

TABLE 6-13. LOGIC MODULE ASSEMBLY - 950-0035
(Sheet 4 of 5)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R71	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R72	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R73	Resistor, 1.5 k Ohm ±5%, 1/4W	100–1543	1
R74	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R77	Resistor, 2 k Ohm ±5%, 1/4W	100–2043	1
R78	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1
R79	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R80	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R81	Resistor, 200 Ohm ±5%, 1/4W	100–2033	1
R82,R83	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R84	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R85 THRU R88	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	4
R89	Resistor, 360 k Ohm ±5%, 1/4W	100–3663	1
R90 THRU R94	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	5
R95	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R96,R97	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R98	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R99	Resistor, 7.5 Meg Ohm ±5%, 1/4W	100–7573	1
R100	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R101,R102	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R103,R104	Resistor, 1.5 k Ohm ±5%, 1/4W	100–1543	2
R105	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R106,R107	Resistor, 1.5 k Ohm ±5%, 1/4W	100–1543	2
R108	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R109	Resistor, 160 k Ohm ±5%, 1/4W	100–1663	1
R110	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R111	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R112	Resistor, 1.5 k Ohm ±5%, 1/4W	100–1543	1
R113 THRU R115	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	3
R116	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1
R117	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R118	Resistor, 30 k Ohm ±5%, 1/4W	100–3053	1
R119,R120	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	2
R121,R122	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R123	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R124	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R125	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R126	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R127	Resistor, 33 Ohm ±5%, 1/4W	100–3323	1
R128	Resistor, 47 Ohm ±5%, 2W, W/W	130–4724	1
R130	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R131	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R132	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1
R133 THRU R135	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	3

TABLE 6–13. LOGIC MODULE ASSEMBLY – 950–0035
(Sheet 5 of 5)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R136	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R137	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R138	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R139	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R140	Resistor, 27 k Ohm ±5%, 1/4W	100–2753	1
R141	Resistor, 15 k Ohm ±5%, 1/4W	100–1553	1
R142	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
U1	Integrated Circuit, RC4559NB, Operational Amplifier, 8–Pin DIP	221–4559	1
U2	Integrated Circuit, MC14040B, CMOS MSI 12–Bit Binary Counter, 16–Pin DIP	220–4040	1
U10	Integrated Circuit, NE565N, Phase–locked Loop Linear, 14–Pin DIP	229–0565	1
U11	Integrated Circuit, TLO74CN, Quad JFET–Input Operational Amplifier, 14–Pin DIP	221–0074	1
U12	Integrated Circuit, LM339AN, Quad Comparator, 14–Pin DIP	221–0339	1
U13	Integrated Circuit, MC14584, Hex Schmitt Trigger, CMOS, 14–Pin DIP	228–4584	1
U14,U15	Integrated Circuit, ULN2004, 7 NPN Darlington Driver Pack, 16–Pin DIP	226–2004	2
U16	Integrated Circuit, MC14584, Hex Schmitt Trigger, CMOS, 14–Pin DIP	228–4584	1
U17	Integrated Circuit, MC14071, OR Gate, CMOS, 14–Pin DIP	225–0005	1
U18	Integrated Circuit, MC14011BCP, Quad 2–Input NAND Gate, CMOS, 14–Pin DIP	228–4011	1
U19	Integrated Circuit, MC14001B, CMOS, Quad 2–Input NOR Gate, 14–Pin DIP	228–4001	1
U20	Integrated Circuit, MC14081, Quad 2–Input AND Gate, CMOS, 14–Pin DIP	225–0008	1
U21,U22	Integrated Circuit, MC14071, OR Gate, CMOS, 14–Pin DIP	225–0005	2
U23,U24	Integrated Circuit, MC14013BCP, Dual D–Type Flip–Flop, CMOS, 14–Pin DIP	228–4013	2
U25	Integrated Circuit, MC14043BP, CMOS, Quad NOR Gate, 16–Pin DIP	220–4043	1
U26	Integrated Circuit, MC14073B, Tripple 3–Input AND Gate, CMOS, 14–Pin DIP	228–4073	1
U27	Integrated Circuit, MC14538B, Dual Retriggerable, Resettable Monostable Multivibrator, CMOS, 16–Pin DIP	228–4538	1
U29	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
U30	Integrated Circuit, LM337L, Adjustable Negative Voltage Regulator, 1.2V to 37V, 0.1 Ampere Maximum, TO–92 Case	220–0337	1
XU1	Socket, 8–Pin DIP	417–0804	1
XU2	Socket, 16–Pin DIP	417–1604	1
XU10 THRU XU13	Socket, 14–Pin DIP	417–1404	4
XU14,XU15	Socket, 16–Pin DIP	417–1604	2
XU16 THRU XU24	Socket, 14–Pin DIP	417–1404	9
XU25	Socket, 16–Pin DIP	417–1604	1
XU26	Socket, 14–Pin DIP	417–1404	1
XU27	Socket, 16–Pin DIP	417–1604	1
W1 THRU W3	Fuseable Link, 22 AWG	601–0022	3
——	Washer, Shoulder, #4	407–0132	1
——	Blank Circuit Board	510–9004	1

TABLE 6–14. PT–90 RECORD PRE–AMPLIFIER MODULE ASSEMBLY – 950–0104
(Sheet 1 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1 THRU C4	Capacitor, Electrolytic, 10 uF, 25V, Non–Polarized	023–1075	1
C5 THRU C8	Capacitor, Mica, 390 pF ±5%, 100V	042–3922	1
C9 THRU C13	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	5
C14	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C15	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C16	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C17,C18	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C19,C20	Capacitor, Ceramic Disc, 10 pF ±10%, 1kV, Non–Polarized	001–1014	2
C21,C22	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C23,C24	Capacitor, Electrolytic, 10 uF, 25V, Non–Polarized	023–1075	2
C25,C26	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	2
C27	Capacitor, Mica, 47 pF ±5%, 500V	040–4713	1
C28	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C29	Capacitor, Mica, 47 pF ±5%, 500V	040–4713	1
C30	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C31	Capacitor, Mica, 1000 pF ±5%, 500V	042–3913	1
C32	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C33	Capacitor, Mica, 1000 pF ±5%, 500V	042–3913	1
C34,C35,C36	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	3
C37	Capacitor, Ceramic Disc, 10 pF ±10%, 1kV, Non–Polarized	001–1014	1
C38	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C39	Capacitor, Ceramic Disc, 10 pF ±10%, 1kV, Non–Polarized	001–1014	1
C40,C41,C42	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	3
C43,C44	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C45,C46	Capacitor, Electrolytic, 4.7 uF, 35V, Low Leakage	024–4753	2
C47,C48	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C49,C50	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C51	Capacitor, Mica, 270 pF ±5%, 300V	041–2722	1
C52,C53	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C54	Capacitor, Electrolytic, 2.2 uF, 50V	020–2264	1
C55	Capacitor, Mylar, 0.22 uF ±10%, 100V	030–2253	1
C56	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C57	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C58	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C59	Capacitor, Mylar, 0.22 uF ±10%, 100V	030–2253	1
C60 THRU C63	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	4
C64	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C65,C66	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	2
C67,C68	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C69	Capacitor, Mylar Film, 0.022 uF ±10%, 100V	031–2243	1
C70	Capacitor, Mylar, 0.22 uF ±10%, 100V	030–2253	1
C71 THRU C74	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	4
D1 THRU D4	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	1
D5,D6	Diode, 1N4737, Zener, 7.5V ±10%, 1W	200–4737	2
D7,D8	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203–4005	2
D9,D10	Diode, 1N34, Germanium, 8.5 mA, 10V	202–0034	2
D11 THRU D14	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	4

TABLE 6–14. PT–90 RECORD PRE–AMPLIFIER MODULE ASSEMBLY – 950–0104
(Sheet 2 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
DS1,DS2	LED, Green, 5300E5, 2.3V @ 50 mA Maximum	323–2206	2
J902,J903	Connector, Audio PC, FEM Series, 3–Pin	418–0051	2
P901	Receptacle, 50–Pin Dual In–line	417–0147	1
Q1,Q2	Transistor, 2N3904, NPN, Silicon, TO–92 Case	211–3904	2
Q3	Transistor, MPS–A14, Silicon, NPN, Darlington, TO–92 Case	211–0014	1
Q4	Field Effect Transistor, J271, P–Channel JFET, TO–92 Case	210–0271	1
R1 THRU R4	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	4
R5	Resistor Network, 10–10 k Ohm 0.5% Resistors, 0.7W Total Dissipation, 16–Pin DIP	226–0392	1
R6,R7	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R8,R9	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	2
R10	Potentiometer, 50 k Ohm ±10%, 3/4W	179–5050	1
R11	Resistor, 120 Ohm ±5%, 1/4W	100–1233	1
R12	Resistor, 1 Meg Ohm ±1%, 1/4W	103–1007	1
R13,R14	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R15,R16	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	2
R17	Potentiometer, 50 k Ohm ±10%, 3/4W	179–5050	1
R18	Resistor, 120 Ohm ±5%, 1/4W	100–1233	1
R19	Resistor, 52.3 k Ohm ±1%, 1/4W	103–5235	1
R20,R21	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	2
R22	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	1
R23	Resistor, 162 k Ohm ±1%, 1/4W	103–1626	1
R24	Resistor, 2.4 k Ohm ±5%, 1/4W	100–2443	1
R25	Resistor, 1 k Ohm ±1%, 1/4W	100–1041	1
R26	Resistor, 9.09 k Ohm ±1%, 1/4W	103–9041	1
R27	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R28	Resistor, 1.5 k Ohm ±5%, 1/4W	100–1543	1
R29	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R30	Resistor, 52.3 k Ohm ±1%, 1/4W	103–5235	1
R31	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R32	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	1
R33	Resistor, 162 k Ohm ±1%, 1/4W	103–1626	1
R34	Resistor, 1 k Ohm ±1%, 1/4W	100–1041	1
R35	Resistor, 9.09 k Ohm ±1%, 1/4W	103–9041	1
R36	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R37	Resistor, 1.5 k Ohm ±5%, 1/4W	100–1543	1
R38,R39	Resistor, 1.21 k Ohm ±1%, 1/4W	103–1214	2
R40,R41	Resistor, 68.1 Ohm ±1%, 1/4W	103–6812	2
R42	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R43 THRU R46	Resistor, 7500 Ohm ±5%, 1/4W	100–7543	4
R47,R48	Potentiometer, 50 k Ohm ±10%, 1/2W	178–5054	2
R49,R50	Resistor, 13 k Ohm ±5%, 1/4W	100–1353	2
R51,R52	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R53 THRU R56	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	4
R57	Resistor, 51 Ohm ±5%, 1/4W	100–5123	1
R58	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1

TABLE 6–14. PT–90 RECORD PRE–AMPLIFIER MODULE ASSEMBLY – 950–0104
(Sheet 3 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R59	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R60,R61	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R62	Resistor, 51 Ohm ±5%, 1/4W	100–5123	1
R63	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R64	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R65	Potentiometer, 100 k Ohm ±10%, 1/2W	178–1064	1
R66,R67	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	2
R68 THRU R71	Resistor, 7.50 k Ohm ±1%, 1/4W	103–7541	4
R72,R73	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	2
R74	Resistor, 20.0 k Ohm ±1%, 1/4W	103–2051	1
R75,R76,R77	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	3
R78	Resistor, 20.0 k Ohm ±1%, 1/4W	103–2051	1
R79	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R80	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R81	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R82	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R83	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R84	Resistor, 51 Ohm ±5%, 1/4W	100–5123	1
R85	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R86	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R87	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R88	Resistor, 51 Ohm ±5%, 1/4W	100–5123	1
R89	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R90	Potentiometer, 100 k Ohm ±10%, 1/2W	178–1064	1
R91	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R92	Resistor, 5.11 k Ohm ±1%, 1/4W	103–5141	1
R93	Resistor, 316 Ohm ±1%, 1/4W	103–3163	1
R94	Resistor, 5.11 k Ohm ±1%, 1/4W	103–5141	1
R95	Resistor, 316 Ohm ±1%, 1/4W	103–3163	1
R96	Resistor, 10 Ohm ±5%, 1/4W	100–1023	1
R97	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R98,R99	Resistor, 1.5 k Ohm ±1%, 1/4W	103–1504	2
R100	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R101	Resistor, 10 Ohm ±5%, 1/4W	100–1023	1
R102	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R103	Resistor, 2 Meg Ohm ±5%, 1/4W	100–2073	1
R104	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R105	Resistor, 178 k Ohm ±1%, 1/4W	103–1761	1
R106	Resistor, 22.6 k Ohm ±1%, 1/4W	103–2265	1
R107	Resistor, 31.6 k Ohm ±1%, 1/4W	100–3151	1
R108	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R109	Resistor, 1 Meg Ohm ±1%, 1/4W	103–1007	1
R110	Resistor, 2.4 k Ohm ±5%, 1/4W	100–2443	1
R111	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R112	Resistor, 510 k Ohm ±5%, 1/4W	100–5163	1
R113	Resistor, 2 Meg Ohm ±5%, 1/4W	100–2073	1

TABLE 6–14. PT–90 RECORD PRE–AMPLIFIER MODULE ASSEMBLY – 950–0104
(Sheet 4 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R114	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R115	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R116,R117	Resistor, 1 Meg Ohm ±1%, 1/4W	103–1007	2
R118	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R119	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R120 THRU R123	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	4
R124	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R125,R126	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	2
R128	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R129	Resistor, 510 k Ohm ±5%, 1/4W	100–5163	1
R130	Resistor, 470 k Ohm ±5%, 1/4W	100–4763	1
R131	Resistor, 15 k Ohm ±5%, 1/4W	100–1553	1
R132	Resistor, 2.26 k Ohm ±1%, 1/4W	103–2264	1
R133	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R134	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R135,R136	Resistor, 2.4 k Ohm ±5%, 1/4W	100–2443	2
TP1 THRU TP4	Terminal, Turret, Double Shoulder	413–1597	4
U1,U2	Integrated Circuit, TLO74CN, Quad JFET–Input Operational Amplifier, 14–Pin DIP	221–0074	2
U3	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U4	Integrated Circuit, LM339AN, Quad Comparator, 14–Pin DIP	221–0339	1
U5	Integrated Circuit, MC14052B, Dual 4–Channel Analog Multiplexers/Demultiplexers, CMOS MSI, 2P4T, 16–Pin DIP	220–4052	1
U6,U7	Integrated Circuit, 2150A, Voltage Controlled Amplifier, 8–Pin SIP	220–2150	2
U8 THRU U11	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	4
U12,U13	Integrated Circuit, 2150A, Voltage Controlled Amplifier, 8–Pin SIP	220–2150	2
U14	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U15	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
U16	Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0337	1
U17	Integrated Circuit, TL311P, JFET–Input Differential Comparator, 8–Pin DIP	220–0311	1
U18	Integrated Circuit, MC14093B, CMOS SSI, Quad 2–Input NAND Schmitt Trigger, 14–Pin DIP	220–4093	1
U19	Integrated Circuit, LF353N, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0353	1
XR5	Socket, 16–Pin DIP	417–1604	1
XU1,XU2	Socket, 14–Pin DIP	417–1404	2
XU3	Socket, 8–Pin DIP	417–0804	1
XU4	Socket, 14–Pin DIP	417–1404	1
XU5	Socket, 16–Pin DIP	417–1604	1
XU8 THRU XU11,XU14, XU17	Socket, 8–Pin DIP	417–0804	6
XU18	Socket, 14–Pin DIP	417–1404	1
XU19	Socket, 8–Pin DIP	417–0804	1
——	Washer, Shoulder, #4 (for U18)	407–0132	2
——	Blank Record Pre–Amplifier Circuit Board	510–9009	1

TABLE 6–15. POWER SUPPLY MODULE ASSEMBLY – 950–0032–001

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1,C2	Capacitor, Electrolytic, 2200 uF, 35V	014–2293	2
C3	Capacitor, Electrolytic, 10 uF ±20%, 50V	023–1076	1
C4	Capacitor, Electrolytic, 4700 uF ±20%, 50V	020–4794	1
C5	Capacitor, Electrolytic, 10,000 uF ±20%, 16V	020–1094	1
C6	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	1
C7,C8	Capacitor, Electrolytic, 1 uF, 50V	024–1064	2
D1 THRU D4	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203–4005	4
D5 THRU D12	Diode, MR502, Silicon, 200V @ 3 Amperes	202–0502	8
D13,D14	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	2
D15	Diode, Zener, 1N4750A, 27V ±10%, 1 Watt	200–0027	1
D16	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	1
E1 THRU E4	Turret Terminal, Double Shoulder	413–1597	4
F1	Fuse, AGC, 1A, 250V, Slow–Blow (for 115 Volt Operation)	334–0100	1
J201	Receptacle, 40–Pin, Dual In–line	417–4041	1
J202	Connector, 9–Pin	418–0900	1
J203	Connector, Header, 3–Pin	417–0003	1
P202	Connector Plug, 9–Pin	417–0059	1
P203	Connector Housing, 3–Pin	417–0003–001	1
Q1	Transistor, 2N3904, Silicon, NPN, TO–92 Case	211–3904	1
Q2	Transistor, TIP120, Silicon, NPN Darlington, 65W @ 255C Case	210–0120	1
Q3	Transistor, 2N3904, Silicon, NPN, TO–92 Case	211–3904	1
Q4	Transistor, TIP125, Silicon, PNP, Darlington, TO–220 Case	210–0125	1
Q5	Transistor, TIP31A, Silicon, NPN, TO–220 AB Case	219–0031	1
R1	Resistor, 470 Ohm ±5%, 1/4W	100–4733	1
R2	Resistor, 68 k Ohm ±5%, 1/4W	100–6853	1
R3	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R4	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R5,R6	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R7	Resistor, 5 Ohm ±1%, 1W, W/W	120–5011	1
R8	Resistor, 15 Ohm ±5%, 1/4W	100–1523	1
R9	Potentiometer, 50 Ohm ±10%, 1/2W	178–5002	1
R11 THRU R14,R16	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	5
S202	Switch, Slide, DPDT, Miniature, 1 Ampere @ 125V ac	345–0126	1
T1	Transformer, Toroid Primary: 115V AC 50/60 Hz @ 0.68 Ampere, 230V AC 50/60 Hz @ 0.34 Ampere Secondary: 1) 20V AC @ 0.40 Ampere, 2) 25V AC @ 1.0 Ampere, 3) 9V AC @ 150 mA	370–4390	1
U1	Integrated Circuit, LM317K, Three–Terminal Adjustable Positive Voltage Regulator, 1.2 to 37V, 1.5 Ampere Maximum, TO–3 Case	227–0318	1
——	Socket, Transistor, TO–3	417–0298	1
——	Socket, Connector	417–0053	6
——	Pins, Crimp Type	417–8766	3
——	AC Power Receptacle, On/Off Power Switch and Fuse Holder	418–0050	1
——	Blank Power Supply Circuit Board	510–9018	1

TABLE 6–16. PT–90 CPU MODULE ASSEMBLY – 950–0101
(Sheet 1 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1,C2	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C3	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C4	Capacitor, Mylar, 0.1 uF ±10%, 100V	030–1053	1
C5,C6	Capacitor, Ceramic Monolithic, 10 pF ±5%, 100V	000–1013	2
C7,C8	Capacitor, Electrolytic, 1 uF, 50V	024–1064	2
C9	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	1
C10 THRU C15	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	6
C17,C18	Capacitor, Electrolytic, 2.2 uF, 25V dc	013–2064	2
C19	Capacitor, Mica, 1000 pF ±1%, 100V	041–1031	1
C20 THRU C24	Capacitor, Electrolytic, 10 uF, 35V	023–1076	5
C25 THRU C59	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	35
C60 THRU C62	Capacitor, Electrolytic, 10 uF, 35V	023–1076	3
C63	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
D1 THRU D4	Diode, 1N34, Germanium, 8.5 mA, 10V	202–0034	4
D5 THRU D13	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	9
D14 THRU D20	Diode, 1N34, Germanium, 8.5 mA, 10V	202–0034	7
D21 THRU D27	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203–4005	7
D28,D29,D30	Diode, 1N34, Germanium, 8.5 mA, 10V	202–0034	3
D31,D32	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	2
J802	Connector, Right Angle, 25–Pin	417–0153	1
P801	Receptacle, 60–Position, Dual In–line	417–0155	1
R1	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R2	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R3	Resistor, 180 k Ohm ±5%, 1/4W	100–1863	1
R5	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R6	Resistor, 120 k Ohm ±5%, 1/4W	100–1263	1
R7	Resistor, 1.5 Meg Ohm ±5%, 1/4W	100–1573	1
R8	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R9	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R10	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R11	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R12	Potentiometer, 50 k Ohm ±10%, 1/2W	178–5054	1
R13	Resistor, 2.2 k Ohm ±5%, 1/4W	100–2243	1
R14	Resistor, 4.7 k Ohm ±5%, 1/4W	100–4743	1
R15	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R16	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R17	Potentiometer, 50 k Ohm ±10%, 1/2W	178–5054	1
R18	Resistor, 2.2 k Ohm ±5%, 1/4W	100–2243	1
R19	Resistor, 4.7 k Ohm ±5%, 1/4W	100–4743	1
R20,R21	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R22	Potentiometer, 5 k Ohm ±20%, 3/4W	178–5044	1
R23	Resistor, 15 k Ohm ±5%, 1/4W	100–1553	1
R24	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R25	Resistor, 10 Ohm ±5%, 1/4W	100–1023	1

TABLE 6–16. PT–90 CPU MODULE ASSEMBLY – 950–0101
(Sheet 2 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R26	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R27	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R28 THRU R33	Resistor, 22 Ohm ±5%, 1/4W	100–2223	6
R34	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R35	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R36	Resistor, 665 Ohm ±1%, 1/4W	103–6653	1
R37	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R38	Resistor, 665 Ohm ±1%, 1/4W	103–6653	1
R39	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R40	Resistor, 383 Ohm ±1%, 1/4W	103–3833	1
R41,R42	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	2
R43 THRU R50	Resistor, 100 Ohm ±5%, 1/4W	100–1033	8
R51	Resistor, 1 Ohm ±5%, 1/4W	100–1013	1
R52	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
RNET1, RNET2	Resistor Network, 9 – 10 k Ohm ±2%, 1/4W Resistors, Single In–Line 10–Pin Package	226–1050	2
S1	Switch, Toggle, 3PST, 0.4 VA Maximum @ 20V ac or dc	340–0095	1
U1,U2	Integrated Circuit, 82C43, Micro Controller Input/Output Expander, CMOS, 24–Pin DIP	220–8243	2
U3	Integrated Circuit, 80C39, Micro Controller, 8–Bit Single–Component, CMOS, 40–Pin DIP	220–8039	1
U4	Integrated Circuit, MC14011BCP, Quad 2–Input NAND Gate, CMOS, 14–Pin DIP	228–4011	1
U5	Integrated Circuit, 82C53, Triple Programmable Interval Timer, 24–Pin DIP	220–8253	1
U6	Integrated Circuit, 74HC373, 8–Bit Latch, Tri–State Output, CMOS, 20–Pin DIP	220–7473	1
U7	Software Kit, PT–90RP	970–0120	1
U8	Integrated Circuit, X2816AD, 2K X 8 Non–Volatile Random–Access–Memory, NMOS, 24–Pin DIP	220–2816	1
U9,U10	Integrated Circuit, MC14051, 8–Bit Analog Multiplexer, CMOS, 16–Pin DIP	220–4051	2
U11	Integrated Circuit, MC14013BCP, Dual D–Type Flip–Flop, CMOS, 14–Pin DIP	228–4013	1
U12	Integrated Circuit, ULN2004, 7 Section NPN Darlington Driver, CMOS, 16–Pin DIP	226–2004	1
U13	Integrated Circuit, MC14013BCP, Dual D–Type Flip–Flop, CMOS, 14–Pin DIP	228–4013	1
U14 THRU U19	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	6
U20,U21	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	2
U22	Integrated Circuit, LM337L, Adjustable Negative Voltage Regulator, 1.2 to 37V, 0.1A Maximum, TO–92 Case	220–0337	1
U23	Integrated Circuit, CD4071B, OR Gate, CMOS, 14–Pin DIP	225–0005	1
Y1	Crystal, 6.144 MHz 0.01% from 05C to +705C, 30 pF Load Capacitance, HC–18 Case	390–0020	1
——	Socket, 8–Pin DIP	417–0804	6
——	Socket, 20–Pin DIP	417–2004	1
——	Socket, 24–Pin DIP	417–2404	4
——	Receptacle, 28–Pin DIP	417–2804	1

TABLE 6–16. PT–90 CPU MODULE ASSEMBLY – 950–0101
(Sheet 3 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
——	Socket, 14–Pin DIP	417–1404	4
——	Socket, 40–Pin DIP	417–4005	1
——	Socket, 16–Pin DIP	417–1604	3
——	Blank CPU Circuit Board	510–9012	1

TABLE 6–17. PT–90 RECORD BIAS MODULE ASSEMBLY – 950–0102
(Sheet 1 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1,C2	Capacitor, Electrolytic, 1 uF, 50V	024–1064	2
C3 THRU C8	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	6
C9,C10	Capacitor, Polyester, 0.0022 uF ±10%, 100V	031–2033	2
C11,C12	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	2
C13,C14	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	2
C15 THRU C21	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	7
C22	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C23	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C24,C25	Capacitor, Electrolytic, 4.7 uF, 35V, Low Leakage	024–4753	2
C26 THRU C29	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	4
C30	Capacitor, Polyester, 0.0022 uF ±10%, 100V	031–2033	1
C31	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C32	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	1
C33	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	1
C34,C35	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C37	Capacitor, Electrolytic, 1O uF, 25V, Non–Polarized	024–1075	1
C38	Capacitor, Mylar Film, 0.022 uF ±10%, 100V	031–2243	1
C39,C40	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C41	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030–1033	1
C42	Capacitor, Mica, 330 pF ±5%, 500V	042–3322	1
C43	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	1
C44,C45	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C46	Capacitor, Mica, 270 pF ±5%, 300V	041–2722	1
C47	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030–1033	1
C48	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	1
C49,C50	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C51	Capacitor, Ceramic Disc, 0.005 uF, 50V	000–5034	1
C52	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	1
C53	Capacitor, Polyester, 0.0022 uF ±10%, 100V	031–2033	1
C54	Capacitor, Ceramic Disc, 0.005 uF, 50V	000–5034	1
C55,C56	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C57	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	1
C58	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C59	Capacitor, Mica, 270 pF ±5%, 300V	041–2722	1
C60	Capacitor, Polyester, 0.0022 uF ±10%, 100V	031–2033	1

TABLE 6–17. PT–90 RECORD BIAS MODULE ASSEMBLY – 950–0102
(Sheet 2 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C61,C62	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C63,C64	Capacitor, Electrolytic, 3.3 uF, 50V, Non–Polarized	024–3364	2
C65	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C66,C67	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C68,C69	Capacitor, Electrolytic, 3.3 uF, 50V, Non–Polarized	024–3364	2
C70,C71	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C72,C73	Capacitor, Electrolytic, 1 uF, 50V	024–1064	2
C74,C75	Capacitor, Mylar Film, 0.047 uF ±10%, 100V	030–4743	2
C78,C79	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	2
C80 THRU C85	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	6
C86,C87	Capacitor, Electrolytic, 10 uF, 25V, Non–Polarized	024–1075	2
C88	Capacitor, Mica, 330 pF ±5%, 500V	042–3322	1
C89	Capacitor, Mica, 270 pF ±5%, 300V	041–2722	1
C90,C91	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C92,C93	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C94,C95	Capacitor, Electrolytic, 4.7 uF, 35V, Low Leakage	024–4753	2
C96,C97	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C98,C99	Capacitor, Electrolytic, 4.7 uF, 35V, Low Leakage	024–4753	2
C100,C101	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C102,C103	Capacitor, Mylar Film, 0.022 uF ±10%, 100V	031–2243	2
C104 THRU C109	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	6
C110	Capacitor, Mylar, 0.01 uF ±10%, 100V	031–1043	1
C111 THRU C113	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	3
C114	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C115,C116	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030–1033	2
C117,C118	Capacitor, Mica, 47 pF ±5%, 500V	040–4713	2
C119	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
D1 THRU D15	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	15
D16,D17	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203–4005	2
D18,D19,D20	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	3
D21,D22	Diode, 1N4737, Zener, 7.5V ±10%, 1W	200–4737	2
D23	Diode, Germanium, 8.5 mA, 10V	202–0034	1
J702	Receptacle, Male, 2–Pin In–line	417–4004	1
P701	Receptacle, 50–Pin Dual In–line	417–0147	1
P702	Jumper, Programmable, 2–Pin	340–0004	1
R1	Resistor, 47 k Ohm ±5%, 1/4W	100–4753	1
R2	Resistor, 27 k Ohm ±5%, 1/4W	100–2753	1
R3	Resistor, 91 k Ohm ±5%, 1/4W	100–9153	1
R4,R5,R6	Resistor, 1 k Ohm ±1%, 1/4W	100–1041	3
R7	Resistor, 47 k Ohm ±5%, 1/4W	100–4753	1
R8	Resistor, 27 k Ohm ±5%, 1/4W	100–2753	1
R9	Resistor, 91 k Ohm ±5%, 1/4W	100–9153	1
R10,R11,R12	Resistor, 1 k Ohm ±1%, 1/4W	100–1041	3
R13,R14	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R15	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R16	Potentiometer, 50 k Ohm ±10%, 1/2W	178–5054	1

TABLE 6–17. PT–90 RECORD BIAS MODULE ASSEMBLY – 950–0102
(Sheet 3 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R17	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R18	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R19	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R20	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R21	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R22,R23	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R24	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R25 THRU R28	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	4
R29	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R30	Potentiometer, 20 k Ohm ±10%, 1/2W	178–2054	1
R31,R32,R33	Resistor, 1 k Ohm ±1%, 1/4W	100–1041	3
R34	Resistor, 169 Ohm ±1%, 1/4W	103–1693	1
R35,R36	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R37	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R38	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R39	Resistor, 5.6 k Ohm ±5%, 1/4W	100–5643	1
R40	Resistor, 150 k Ohm ±1%, 1/4W	103–1561	1
R41	Resistor, 61.9 k Ohm ±1%, 1/4W	103–6195	1
R42	Resistor, 102 k Ohm ±1%, 1/4W	103–1026	1
R43,R44	Resistor, 4.87 k Ohm ±1%, 1/4W	103–4874	2
R45	Resistor, 14.3 k Ohm ±1%, 1/4W	103–1435	1
R46	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R47	Resistor, 61.9 k Ohm ±1%, 1/4W	103–6195	1
R48	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R49	Resistor, 66.5 k Ohm ±1%, 1/4W	103–6655	1
R50,R51	Resistor, 88.7 k Ohm ±1%, 1/4W	103–8875	2
R52	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	1
R53	Potentiometer, 20 k Ohm ±10%, 1/2W	178–2054	1
R54	Potentiometer, 50 k Ohm ±10%, 1/2W	178–5054	1
R55	Resistor, 2 k Ohm ±5%, 1/4W	100–2043	1
R56	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R57	Resistor, 221 k Ohm ±1%, 1/4W	103–2216	1
R58	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R59	Resistor, 221 k Ohm ±1%, 1/4W	103–2216	1
R60,R61	Resistor, 59.0 k Ohm ±1%, 1/4W	103–5905	2
R62	Resistor, 2.4 k Ohm ±5%, 1/4W	100–2443	1
R63	Potentiometer, 20 k Ohm ±10%, 1/2W	178–2054	1
R64	Resistor, 19.1 k Ohm ±1%, 1/4W	103–1915	1
R65 THRU R68	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	4
R69	Resistor, 1 Ohm ±5%, 1/4W	100–1013	1
R70	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R71	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R72	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R73	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R74	Resistor, 300 k Ohm ±5%, 1/4W	100–3063	1

TABLE 6–17. PT–90 RECORD BIAS MODULE ASSEMBLY – 950–0102
(Sheet 4 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R75	Resistor, 150 k Ohm ±5%, 1/4W	100–1563	1
R76	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R77	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R78	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R79	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R80	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R81	Resistor, 20 k Ohm ±5%, 1/4W	100–2053	1
R82	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R83	Resistor, 300 k Ohm ±5%, 1/4W	100–3063	1
R84	Resistor, 150 k Ohm ±5%, 1/4W	100–1563	1
R85	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R86	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R87	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R88 THRU R93	Potentiometer, 100 k Ohm ±10%, 1/2W	177–1064	6
R94	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R95,R96	Resistor, 866 Ohm ±1%, 1/4W	103–8663	2
R97	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R98,R99	Resistor, 316 Ohm ±1%, 1/4W	103–3163	2
R100,R101	Resistor, 100 Ohm ±1%, 1/4W	100–1031	2
R102	Resistor, 10.2 k Ohm ±1%, 1/4W	103–1025	1
R103	Resistor, 4.42 k Ohm ±1%, 1/4W	103–4441	1
R104	Resistor, 10.2 k Ohm ±1%, 1/4W	103–1025	1
R105	Resistor, 4.42 k Ohm ±1%, 1/4W	103–4441	1
R106	Resistor, 33 Ohm ±5%, 1/4W	103–3323	1
R107	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R108	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R109	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R110	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R111	Potentiometer, 100 k Ohm ±10%, 1/2W	179–1065	1
R112	Resistor, 10.2 k Ohm ±1%, 1/4W	103–1025	1
R113	Resistor, 4.42 k Ohm ±1%, 1/4W	103–4441	1
R114	Resistor, 10.2 k Ohm +1%, 1/4W	103–1025	1
R115	Resistor, 4.42 k Ohm ±1%, 1/4W	103–4441	1
R116	Resistor, 124 Ohm ±1%, 1/4W	103–1241	1
R117	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R118	Resistor, 33 Ohm ±5%, 1/4W	103–3323	1
R119	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R120	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R121	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1
R122	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R123	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1
R124	Resistor, 200 k Ohm ±5%, 1/4W	100–2063	1
R125,R126	Resistor, 47 Ohm ±5%, 3 1/4W W/W	132–4721	2
R127	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R128	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R129	Resistor Network, 9 – 10 k Ohm ±2%, 1/4W Resistors, Single In–Line 10–Pin Package	226–1050	1

TABLE 6–17. PT–90 RECORD BIAS MODULE ASSEMBLY – 950–0102
(Sheet 5 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R130	Resistor, 2.32 k Ohm ±1%, 1/4W	103–2341	1
R131,R132	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R133	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R134,R135	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R136,R137	Resistor, 270 Ohm ±5%, 1/4W	100–2733	2
R138	Resistor, 10K Ohm ±5%, 1/4W	100–1053	1
U1	Integrated Circuit, MC14053B, Analog Multiplexers/Demultiplexers, CMOS, 16–Pin DIP	220–4053	1
U2	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U3,U4	Integrated Circuit, NE5532AP, Dual Low Noise Operational Amplifier, 8–Pin DIP	221–5532–001	2
U5	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U6	Integrated Circuit, MC14053B, Analog Multiplexers/Demultiplexers, CMOS MSI, 16–Pin DIP	220–4053	1
U7	Integrated Circuit, NE5532AP, Dual Low Noise Operational Amplifier, 8–Pin DIP	221–5532–001	1
U8	Integrated Circuit, MC14040B, CMOS, 12–Bit Binary Counter, 16–Pin DIP	220–4040	1
U9	Integrated Circuit, CD4071B, Quad 2–Input OR Gate, CMOS, 14–Pin DIP	225–0005	1
U10,U11	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	2
U12	Integrated Circuit, MC14040B, CMOS, 12–Bit Binary Counter, 16–Pin DIP	220–4040	1
U13	Integrated Circuit, MF6–CN100, 6th Order Butterworth Low–Pass Filter/Amplifier, 14–Pin DIP	229–0006	1
U14	Integrated Circuit, MC14053B, Analog Multiplexers/Demultiplexers, CMOS, 16–Pin DIP	220–4053	1
U15	Integrated Circuit, MC14040B, CMOS MSI, 12–Bit Binary Counter, 16–Pin DIP	220–4040	1
U16	Integrated Circuit, MC14073B, Tripple 3–Input AND Gate, CMOS, 14–Pin DIP	228–4073	1
U17	Integrated Circuit, MC14011BCP, Quad 2–Input NAND Gate, CMOS, 14–Pin DIP	228–4011	1
U18	Integrated Circuit, MC14013BCP, Dual D–Type Flip–Flop, CMOS, 14–Pin DIP	228–4013	1
U19	Integrated Circuit, MC14584, Hex Schmitt Trigger, CMOS, 14–Pin DIP	228–4584	1
U20	Integrated Circuit, MF6–CN100, 6th Order Butterworth Low–Pass Filter/Amplifier, 14–Pin DIP	229–0006	1
U21	Integrated Circuit, ULN2003A, 7 Section NPN Darlington Driver, CMOS, 16–Pin DIP	229–2003	1
U23	Integrated Circuit, MC14538B, Dual Retriggerable, Resettable Monostable Multivibrator, CMOS, 16–Pin DIP	228–4538	1
U24	Integrated Circuit, NE5532AP, Dual Low Noise Operational Amplifier, 8–Pin DIP	221–5532–001	1
U25	Integrated Circuit, TL072CP, Dual JFET–Input Operational Amplifier, 8–Pin DIP	221–0072	1
U26	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
U27	Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0337	1
U28	Integrated Circuit, LM317LZ, Adjustable Positive Voltage Regulator, 1.2 to 37V @ 0.1 Ampere, TO–92 Case	220–0317	1
U29	Integrated Circuit, LM337L, Adjustable Negative Voltage Regulator, 1.2 to 37V, 0.1A Maximum, TO–92 Case	220–0337	1

TABLE 6–17. PT–90 RECORD BIAS MODULE ASSEMBLY – 950–0102
(Sheet 6 of 6)

REF. DES.	DESCRIPTION	PART NO.	QTY.
U30	Integrated Circuit, MC14052B, Dual 4–Channel Analog Multiplexers/Demultiplexers, CMOS, 2P4T, 16–Pin DIP	220–4052	1
U31,U32	Integrated Circuit, TLO74CN, Quad JFET–Input Operational Amplifier, 14–Pin DIP	221–0074	2
XU1	Socket, 16–Pin DIP	417–1604	1
XU2 THRU XU5	Socket, 8–Pin DIP	417–0804	4
XU6	Socket, 16–Pin DIP	417–1604	1
XU7	Socket, 8–Pin DIP	417–0804	1
XU8	Socket, 16–Pin DIP	417–1604	1
XU9	Socket, 14–Pin DIP	417–1404	1
XU10,XU11	Socket, 8–Pin DIP	417–0804	2
XU12	Socket, 16–Pin DIP	417–1604	1
XU13	Socket, 14–Pin DIP	417–1404	1
XU14,XU15	Socket, 16–Pin DIP	417–1604	2
XU16 THRU XU20	Socket, 14–Pin DIP	417–1404	5
XU21,XU23	Socket, 16–Pin DIP	417–1604	2
XU24,XU2	Socket, 8–Pin DIP	417–0804	2
XU30	Socket, 16–Pin DIP	417–1604	1
XU31,XU32	Socket, 14–Pin DIP	417–1404	2
——	Blank Record Bias Circuit Board	510–9014	1

TABLE 6–18. PLAYBACK MOTHERBOARD ASSEMBLY – 910–9006

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Electrolytic, 100 uF, 50V	020–1083	1
J104	Connector Header, 20–Pin In–Line	417–0200	0.25
J105	Connector Header, 16–Pin Dual In–line	417–1603	1
J106	Connector Header, 26–Pin Dual In–line	417–2600	1
J107	Connector Header, 5–Pin, Right Angle	417–4000–002	1
J108	Connector Header, 26–Pin Dual In–line	417–2600	1
J109 THRU J117	Receptacle, Single Pin	417–0071–001	9
J201	Connector Header, 40–Pin Dual In–line	417–0134	1
J301,J401	Connector Header, 50–Pin Dual In–line	417–0146	2
R1	Resistor, 150 Ohm ±5%, 1/4W	100–1533	1
R2,R3	Resistor, 68 Ohm ±5%, 2W	132–6832	2
——	Blank Circuit Board	510–9006	1

TABLE 6–19. RECORD/PLAYBACK MOTHERBOARD ASSEMBLY – 910–9013
(Sheet 1 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
D1	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203–4005	1
J104	Connector Header, 20–Pin In–Line	417–0200	0.25
J105	Connector Header, 16–Pin Dual In–line	417–1603	1
J106	Connector Header, 26–Pin Dual In–line	417–2600	1

TABLE 6–19. RECORD/PLAYBACK MOTHERBOARD ASSEMBLY – 910–9013
(Sheet 2 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
J107	Connector Header, 5–Pin, Right Angle	417–4000–002	1
J108	Connector Header, 26–Pin Dual In–line	417–2600	1
J109 THRU J125	Receptacle, Single Pin	417–0071–001	18
J201	Connector Header, 40–Pin Dual In–line	417–0134	1
J301,J401, J701	Connector Header, 50–Pin Dual In–line	417–0146	3
J801	Header Assembly, Shrouded, 60–Pin Dual In–line	417–0156	1
J901	Connector Header, 50–Pin Dual In–line	417–0146	1
R1	Resistor, 150 Ohm ±5%, 1/4W	100–1533	1
——	Blank Circuit Board	510–9013	1

TABLE 6–20. PT–90 FRONT PANEL STATUS CIRCUIT BOARD ASSEMBLY –910–9003–1

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C2	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C3	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C4	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C5	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
D1 THRU D4	Diode, Zener, 1N4742A, 12V ±5%, 1W	200–4742	4
DS1 THRU DS4	LED, Green, MV54173, Light Intensity I	320–0016	4
DS5, DS6	LED, Red, MV57173, Light Intensity G	320–0017	2
DS7	LED, Multicolor, HDSP4836, 10–Element Bar Graph Array	320–0013	1
DS8	Light Emitting Diode, LN543RKN8, Red, Four Digit Seven Segment Display	320–0036	1
J501	Connector Header, 26–Pin Dual In–Line	417–2600	1
J502	Connector Header, 20–Pin In–Line	417–0200	0.5
R1	Resistor, 3.92 k Ohm ±1%, 1/4W	103–3924	1
R2 THRU R4	Resistor, 100 k Ohm ±1%, 1/4W	103–1062	3
R5	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	1
R6	Resistor, 8.06 k Ohm ±1%, 1/4W	103–8064	1
R7	Resistor, 1.24 k Ohm ±1%, 1/4W	103–1244	1
R8	Resistor, 100 Ohm ±1%, 1/4W	100–1031	1
R9	Resistor, 316 Ohm ±1%, 1/4W	103–3163	1
R10	Resistor, 1 k Ohm ±1%, 1/4W	100–1041	1
R11 THRU R13	Resistor, 10 k Ohm ±1%, 1/4W	100–1051	3
R14	Resistor, 3.92K Ohm ±1%, 1/4W	103–3924	1
RN–1	Resistor Network, 7 resistors, 1 k Ohm ±2%, 8–Pin Single–In–line Package	226–1032	1
U1	Integrated Circuit, LM3914N, Dot/Bar Display Driver, 18–Pin DIP	229–3914	1
U2	Integrated Circuit, 1CM7217CIPI, 4–Digit (LED) Presettable Up/Down Counter, 28–Pin DIP	220–7217	1
U3	Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2 to 37V, 0.1A Maximum, TO–92 Case	220–0337	1
XU1	Socket, 18–Pin DIP	417–1804	1
XU2	Socket, 28–Pin DIP	417–2804	1
——	Blank Circuit Board	510–9003–1	1

TABLE 6–21. PT–90 RECORD/PLAYBACK FRONT PANEL CIRCUIT BOARD ASSEMBLY – 910–9011 (Sheet 1 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C2,C3	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C4	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C5,C6	Capacitor, Electrolytic, 10 uF, 35V	023–1076	2
C7	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C8	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C9	Capacitor, Electrolytic, 4.7 uF, 35V, Low Leakage	024–4753	1
C10	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C11	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C12	Capacitor, Electrolytic, 100 uF, 25V	024–1084	1
C13,C14	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
D1,D2	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	2
D3	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203–4005	1
DS1 THRU DS4	LED, Green, MV54173, Light Intensity I	320–0016	4
DS5,DS6	LED, Red, MV57173, Light Intensity G	320–0017	2
DS7	LED, Multicolor, HDSP–4836, 10–Element Bar Graph Array	320–0013	1
DS8	LED, Green, MV54164, High Efficiency 10–Segment Bar Graph Array	320–4164	1
DS9	LED, Red, MV57164, High Efficiency 10–Segment Bar Graph Array	320–7164	1
DS10	LED, Green, MV54164, High Efficiency 10–Segment Bar Graph Array	320–4164	1
DS11	LED, Red, MV57164, High Efficiency 10–Segment Bar Graph Array	320–7164	1
DS12	Display, 4–Digit Dot Matrix, Red, PD3535	320–0020	1
J501	Receptacle, Male, 26–Pin Dual In–Line	417–2600	1
J502	Receptacle, Male, 20–Pin In–Line	417–0200	1
J503	Receptacle, Male, 26–Pin Dual In–Line	417–2600	1
R1	Resistor, 8.06 k Ohm ±1%, 1/4W	103–8064	1
R2	Resistor, 1.24 k Ohm ±1%, 1/4W	103–1244	1
R3	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R4,R5	Resistor, 1.21 k Ohm ±1%, 1/4W	103–1214	2
R6	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R7	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R8	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R9	Resistor, 330 k Ohm ±5%, 1/4W	100–3363	1
R10	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R11	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R12	Resistor, 1.8 k Ohm ±5%, 1/4W	100–1843	1
R13,R14	Resistor, 1.21 k Ohm ±1%, 1/4W	103–1214	2
R15	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R16	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R17	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R18	Resistor, 330 k Ohm ±5%, 1/4W	100–3363	1
R19	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R20	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R21	Resistor, 1.8 k Ohm ±5%, 1/4W	100–1843	1
R22	Resistor, 82 Ohm ±5%, 1/2W	110–8223	1
R23	Resistor, 1.02 k Ohm ±1%, 1/4W	103–1024	1
R24	Resistor, 118 Ohm ±1%, 1/4W	100–1111	1
R25	Resistor, 698 Ohm ±1%, 1/4W	103–6983	1
R26	Resistor, 221 Ohm ±1%, 1/4W	103–2213	1
R27	Resistor, 280 Ohm ±1%, 1/4W	103–2803	1

TABLE 6–21. PT–90 RECORD/PLAYBACK FRONT PANEL CIRCUIT BOARD ASSEMBLY – 910–9011 (Sheet 2 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R28,R29,R30	Resistor, 270 Ohm ±5%, 1/4W	100–2733	3
R31	Resistor, 47 k Ohm ±5%, 1/4W	100–4753	1
R32,R33	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R34	Resistor, 1 Ohm ±5%, 1/4W	100–1013	1
R35,R36	Resistor, 220 Ohm ±5%, 1/2W	110–2233	2
R37,R38	Resistor, 680 Ohm ±5%, 1/2W	110–6833	2
RN–1	Resistor Network, 7 resistors, 1 k Ohm ±2%, 8–Pin Single–In–line Package	226–1032	1
S1 THRU S10	Switch, Push, Illuminated, S120601H1, Contacts: SPST, N.O., 24V ac at 125 mA Nominal	340–0107	10
U1	Integrated Circuit, LM3914N, Dot/Bar Display Driver, 18–Pin DIP	229–3914	1
U2 THRU U	Integrated Circuit, LM3916N, Dot/Bar Display Driver, 18–Pin DIP	220–3916	4
U6	Integrated Circuit, LM339AN, Quad Comparator, 14–Pin DIP	221–0339	1
U7	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
XU1 THRU XU5	Socket, 18–Pin DIP	417–1804	5
XU6	Socket, 14–Pin DIP	417–1404	1
——	Blank Circuit Board	510–9011	1

TABLE 6–22. MOTOR CONTROL CIRCUIT BOARD ASSEMBLY – 910–9005 (Sheet 1 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C2	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C3,C4	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C5,C6	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040–1022	2
C7,C8	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C9	Capacitor, Mylar Film, 0.22 uF ±10%, 100V	030–2253	1
C10	Capacitor, Mylar Film, 0.01 uF ±10%, 100V	031–1043	1
C11	Capacitor, Electrolytic, 1 uF, 50V	024–1064	1
C12,C13,C14	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	3
C15	Capacitor, Mylar Film, 0.01 uF ±10%, 100V	031–1043	1
C16 THRU C19	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	4
C20	Capacitor, Mylar Film, 0.01 uF ±10%, 100V	031–1043	1
C21	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1
C22	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C23,C24,C25	Capacitor, Electrolytic, 10 uF, 35V	023–1076	3
C26	Capacitor, Electrolytic, 3.3 uF, 50V	020–3363	1
C27,C28	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C29	Capacitor, Electrolytic, 33 uF, 35V	024–3374	1
C30,C31	Capacitor, Mica, 22 pF ±5%, 500V	040–2213	2
C32 THRU C37	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	6
C38	Capacitor, Electrolytic, 10 uF, 35V	023–1076	1

TABLE 6–22. MOTOR CONTROL CIRCUIT BOARD ASSEMBLY – 910–9005
(Sheet 2 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C39,C40	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	2
C41	Capacitor, Electrolytic, 100 uF, 50V	020–1083	1
C42	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003–1054	1
C43	Capacitor, Ceramic, 0.001 uF ±10%, 200V	030–1033	1
D1 THRU D4	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	4
D5	Diode, 1N34, Germanium, 8.5 mA, l0V	202–0034	1
D6 THRU D8, D11 THRU D14	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203–4148	7
J601	Connector, Header, 20–Pin In–Line	417–0200	0.6
J602	Connector, Header, 8–Pin Dual In–line	417–1603	1
Q1	Transistor, TIP120, NPN Darlington–Connected Silicon Power, 65W @ 255C Case	210–0120	1
Q2,Q3,Q4	Transistor, TIP32A, Silicon, PNP, TO–220 AB Case	218–0032	3
Q5,Q6,Q7	Transistor, MPS–A14, Silicon, NPN, Darlington TO–92 Case	211–0014	3
Q8	Transistor, 2N3906, Silicon, PNP, TO–92 Case	210–3906	1
R1	Resistor, 2.7 k Ohm ±5%, 1/4W	100–2743	1
R2	Resistor, 100 Ohm ±5%, 1/4W	100–1033	1
R3	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R5,R6	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R7,R8,R9	Resistor, 22.1 k Ohm ±1%, 1/4W	103–2211	3
R10	Resistor, 470 k Ohm ±5%, 1/4W	100–4763	1
R11	Resistor, 330 k Ohm ±5%, 1/4W	100–3363	1
R12	Resistor, 30 k Ohm ±5%, 1/4W	100–3053	1
R13	Resistor, 330 k Ohm ±5%, 1/4W	100–3363	1
R14	Resistor, 33 k Ohm ±5%, 1/4W	100–3353	1
R15	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R16	Potentiometer, 500 Ohm, 1/2W	178–5030	1
R17	Resistor, 1 Ohm ±1%, 1W	120–1013	1
R18	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R19,R20	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R21	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R22	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1
R23	Resistor, 51 k Ohm ±5%, 1/4W	100–5153	1
R24	Resistor, 220 k Ohm ±5%, 1/4W	100–2263	1
R25,R26	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R27	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R28	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R29,R30	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	2
R31	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R32,R33,R34	Resistor, 5.1 k Ohm ±5%, 1/4W	100–5143	3
R35	Resistor, 470 Ohm ±5%, 1/2W	110–4733	1
R36	Resistor, 47 Ohm ±5%, 1/2W	110–4723	1
R37,R38	Resistor, 470 Ohm ±5%, 1/2W	110–4733	2
R39	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R40	Resistor, 1 k Ohm ±5%, 1/4W	100–1043	1
R41	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R42	Resistor, 24 k Ohm ±5%, 1/4W	100–2453	1
R43	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1

TABLE 6-22. MOTOR CONTROL CIRCUIT BOARD ASSEMBLY - 910-9005
(Sheet 3 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R44	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	1
R45	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R46	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R47	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R48	Resistor, 510 k Ohm ±5%, 1/4W	100–5163	1
R50	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1
R51,R52	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R54	Resistor, 10 Meg Ohm ±5%, 1/4W	100–1083	1
R56	Resistor, 68 k Ohm ±5%, 1/4W	100–6853	1
R57	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R58	Resistor, 1 Meg Ohm ±5%, 1/4W	100–1073	1
R59,R60,R61	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	3
R62	Resistor, 300 Ohm ±5%, 2W, W/W	130–3004	1
R63	Resistor, 316 Ohm ±1%, 1/4W	103–3163	1
R64	Resistor, 100 Ohm ±1%, 1/4W	100–1031	1
R65	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	1
R66,R67	Resistor, 10 k Ohm ±5%, 1/4W	100–1053	2
R68,R69,R70	Resistor, 100 k Ohm ±5%, 1/4W	100–1063	3
R71	Resistor, 9.1 k Ohm ±5%, 1/4W	100–9143	1
U1	Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case	227–0317	1
U2	Integrated Circuit, LM358N, Dual Operational Amplifier, 8–Pin DIP	221–0358	1
U3	Integrated Circuit, MC14528BCP, Dual Monostable Multivibrator, CMOS, 16–Pin DIP	224–4528	1
U4	Integrated Circuit, MC14011BCP, Quad 2–Input NAND Gate, CMOS, 14–Pin DIP	228–4011	1
U5	Integrated Circuit, MC54/74HC195, 4–Bit Universal Shift Register, CMOS, 16–Pin DIP	220–0195	1
U6	Integrated Circuit, LM358N, Dual Operational Amplifier, 8–Pin DIP	221–0358	1
U7	Integrated Circuit, LM339AN, Quad Comparator, 14–Pin DIP	221–0339	1
U8	Integrated Circuit, MC14040BCP, 12–Bit Binary Counter, CMOS, 16–Pin DIP	220–4040	1
U9	Integrated Circuit, MC14013BCP, Dual D–Type Flip–Flop, CMOS, 14–Pin DIP	228–4013	1
U10	Integrated Circuit, MC14053B, Analog Multiplexers/Demulti–plexers, CMOS, 16–Pin DIP	220–4053	1
U11	Integrated Circuit, MC14060B, 14–Bit Binary Counter and Oscillator, CMOS, 16–Pin DIP	220–4060	1
U12	Integrated Circuit, CD4027BE, Dual J–K Master–Slave Flip–Flop, CMOS, 16–Pin DIP	225–0003	1
U13	Integrated Circuit, MC14052B, Dual 4–Channel Analog Multi–plexers/Demultiplexers, CMOS, 2P4T, 16–Pin DIP	220–4052	1
U14	Integrated Circuit, MC14040BCP, 12–Bit Binary Counter, CMOS, 16–Pin DIP	220–4040	1
U15	Integrated Circuit, ULN2004, 7 NPN Darlington Driver Pack, 16–Pin DIP	226–2004	1
XU2	Socket, 8–Pin DIP	417–0804	1
XU3	Socket, 16–Pin DIP	417–1604	1
XU4	Socket, 14–Pin DIP	417–1404	1
XU5	Socket, 16–Pin DIP	417–1604	1
XU6	Socket, 8–Pin DIP	417–0804	1

TABLE 6–22. MOTOR CONTROL CIRCUIT BOARD ASSEMBLY – 910–9005
(Sheet 4 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
XU7	Socket, 14–Pin DIP	417–1404	1
XU8	Socket, 16–Pin DIP	417–1604	1
XU9	Socket, 14–Pin DIP	417–1404	1
XU10 THRU XU15	Socket, 16–Pin DIP	417–1604	6
Y1	Crystal, 460.80 kHz ±0.01% from 0°C to 50°C, R/DT Cut, NE33D Case	390–0019	1
——	Blank Circuit Board	510–9005	1

TABLE 6–23. PT–90 MOTOR ASSEMBLY – 950–0037

REF. DES.	DESCRIPTION	PART NO.	QTY.
M1	Motor, DC Servo Operating Supply: +24V ±1.2V dc, +5V ±0.2V dc Tachometer: 80 Hz per 1 RPS Operating Torque: 10 oz./in. Maximum Operating Current: 1.1A Maximum Operating Speed: Programmable Model: 58FPAK8003	380–0009	1
——	Bearing, Ball, 609ZZ (Upper Bearing) Outside Diameter: 0.9348 Inches (2.37 cm) Inside Diameter: 0.355 Inches (0.902 cm) Height: 0.275 Inches (0.698 cm)	442–0609	1
——	Bearing, Ball, 699ZZ (Lower Bearing) Outside Diameter: 0.7873 Inches (1.99 cm) Inside Diameter: 0.355 Inches (0.902 cm) Height: 0.2346 Inches (0.596 cm)	442–1023	1
——	Connector Housing, 12–Pin	417–1202	1
——	Pins, Crimp Type	417–8766	11

TABLE 6–24. PT–90 PLAYBACK CABLE ASSEMBLY – 940–0030

REF. DES.	DESCRIPTION	PART NO.	QTY.
P104	Connector Housing, 5–Pin In–line	417–0165	1
P105	Connector, 16–Pin Dual In–line	417–0131	1
P106,P501	Connector, Ribbon Cable, 26–Pin Dual In–line	418–2600	2
P502	Connector Housing, 10–Pin	417–0148	1
P602	Connector, 16–Pin Dual In–line	417–0131	1
——	Pins, Crimp Type	417–8766	13
——	Pins, Connector	417–0142	9

TABLE 6–25. PT–90 RECORD/PLAYBACK CABLE ASSEMBLY – 940–0032

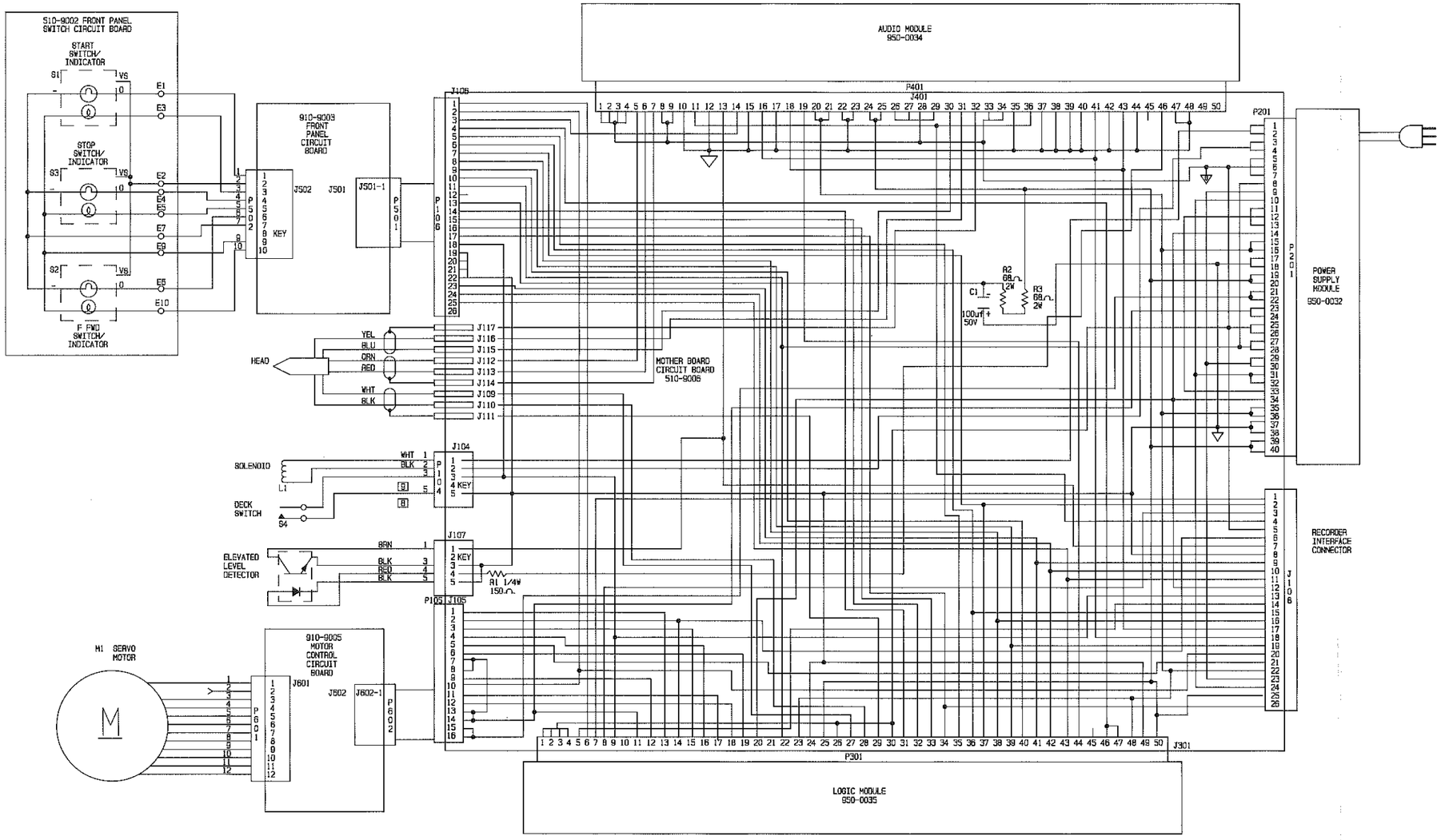
REF. DES.	DESCRIPTION	PART NO.	QTY.
P104	Connector Housing, 5–Pin In–line	417–0165	1
P105	Connector, 16–Pin Dual In–line	417–0131	1
P106,P108, P501	Connector, Ribbon Cable, 26–Pin Dual In–line	418–2600	3
P502	Plug, Housing, 12–Pin	417–1202	1
P503	Connector, Ribbon Cable, 26–Pin Dual In–line	418–2600	1
P602	Connector, 16–Pin Dual In–line	417–0131	1
——	Pins, Crimp Type	417–8766	17

SECTION VII
DRAWINGS

7–1. INTRODUCTION.

7–2. This section provides assembly drawings, wiring diagrams, and schematic diagrams as listed below for the Broadcast Electronics PT–90 series cartridge machines.

FIGURE	TITLE	NUMBER
7–1	PT–90 SERIES PLAYBACK UNIT OVERALL SCHEMATIC DIAGRAM	SD900–9000–000, –300, 900–9002–000, –300
7–2	PT–90 SERIES RECORD/PLAYBACK UNIT OVERALL SCHEMATIC DIAGRAM	SD900–9003–000, –300
7–3	PT–90 SERIES HEAD TO MOTHERBOARD WIRING DIAGRAM	597–9000–100
7–4	PT–90 SERIES PLAYBACK UNIT ASSEMBLY DIAGRAM	AD950–9000
7–5	PT–90 SERIES RECORD/PLAYBACK UNIT ASSEMBLY DIAGRAM	597–9000–200
7–6	PLAYBACK UNIT MOTHERBOARD ASSEMBLY DIAGRAM	AC910–9006
7–7	RECORD/PLAYBACK UNIT MOTHERBOARD SCHEMATIC DIAGRAM	SD910–9013
7–8	RECORD/PLAYBACK UNIT MOTHERBOARD ASSEMBLY DIAGRAM	AD910–9013
7–9	PLAYBACK UNIT FRONT PANEL CIRCUIT BOARD SCHEMATIC DIAGRAM	SC910–9003–1
7–10	PLAYBACK UNIT FRONT PANEL CIRCUIT BOARD ASSEMBLY DIAGRAM	AC910–9003–1
7–11	RECORD/PLAYBACK UNIT FRONT PANEL CIRCUIT BOARD SCHEMATIC DIAGRAM	SD910–9011
7–12	RECORD/PLAYBACK UNIT FRONT PANEL CIRCUIT BOARD ASSEMBLY DIAGRAM	AC910–9011
7–13	AUDIO MODULE SCHEMATIC DIAGRAM	SD950–0033/ –0034
7–14	AUDIO MODULE ASSEMBLY DIAGRAM	AD950–0033/ –0034
7–15	LOGIC MODULE SCHEMATIC DIAGRAM	SD950–0035
7–16	LOGIC MODULE ASSEMBLY DIAGRAM	AD950–0035
7–17	MOTOR CONTROL CIRCUIT BOARD SCHEMATIC DIAGRAM	SD910–9005
7–18	MOTOR CONTROL CIRCUIT BOARD ASSEMBLY DIAGRAM	AC910–9005
7–19	POWER SUPPLY MODULE SCHEMATIC DIAGRAM	SC950–0032/–001
7–20	POWER SUPPLY MODULE ASSEMBLY DIAGRAM	AD950–0032/–001
7–21	CPU MODULE SCHEMATIC DIAGRAM	SD950–0101



P105 TO P602
1. MOTOR RUN
2. MOTOR AT SPEED
3. MOTOR OVERCURRENT
4. TACH OUT
5. MOTOR CURRENT SAMPLE
6. MOTOR RESET
7. POWER SUPPLY GROUND
8. POWER SUPPLY GROUND
9. F FWD MODE
10. SERVO ERROR
11. VARISPEED MODE
12. VARISPEED INPUT 9600Hz
13. POWER SUPPLY GROUND
14. POWER SUPPLY GROUND
15. +28V
16. +28V

P601		
PIN	COLOR	FUNCTION
1.	PINK	+5V
2.		
3	GRN	GND
4.	ORN	TACH HIGH
5.	VIO	TACH LOW
6.	LT.BLU	HALL 2
7.	RED	HALL 3
8.	GRY	HALL 1
9.	BRN	STATOR 1
10.	BLU	STATOR 2
11.	YEL	STATOR 3
12.	WHT	STATOR COM

P106 TO P105
1. VARISPEED IND
2. SERVO IND
3. PHASE DISPLAY
4. +12V
5. START COMMAND
6. START LIGHT
7. STOP COMMAND
8. STOP LIGHT
9. FF COMMAND
10. FF LIGHT
11. +28V LAMP SUPPLY
12. GROUND
13. -22V I LIMITED
14. DATA IND
15. TERT IND
16. SEC IND
17. AUDIO IND
18. CART PRESENT
19. GROUND
20. GROUND
21. GROUND
22. GROUND
23. TIMER FREEZE/COUNT
24. TIMER RESET
25. TIMER 1Hz INPUT
26. -5V

TOLERANCE (DECIMAL) U.O.B.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

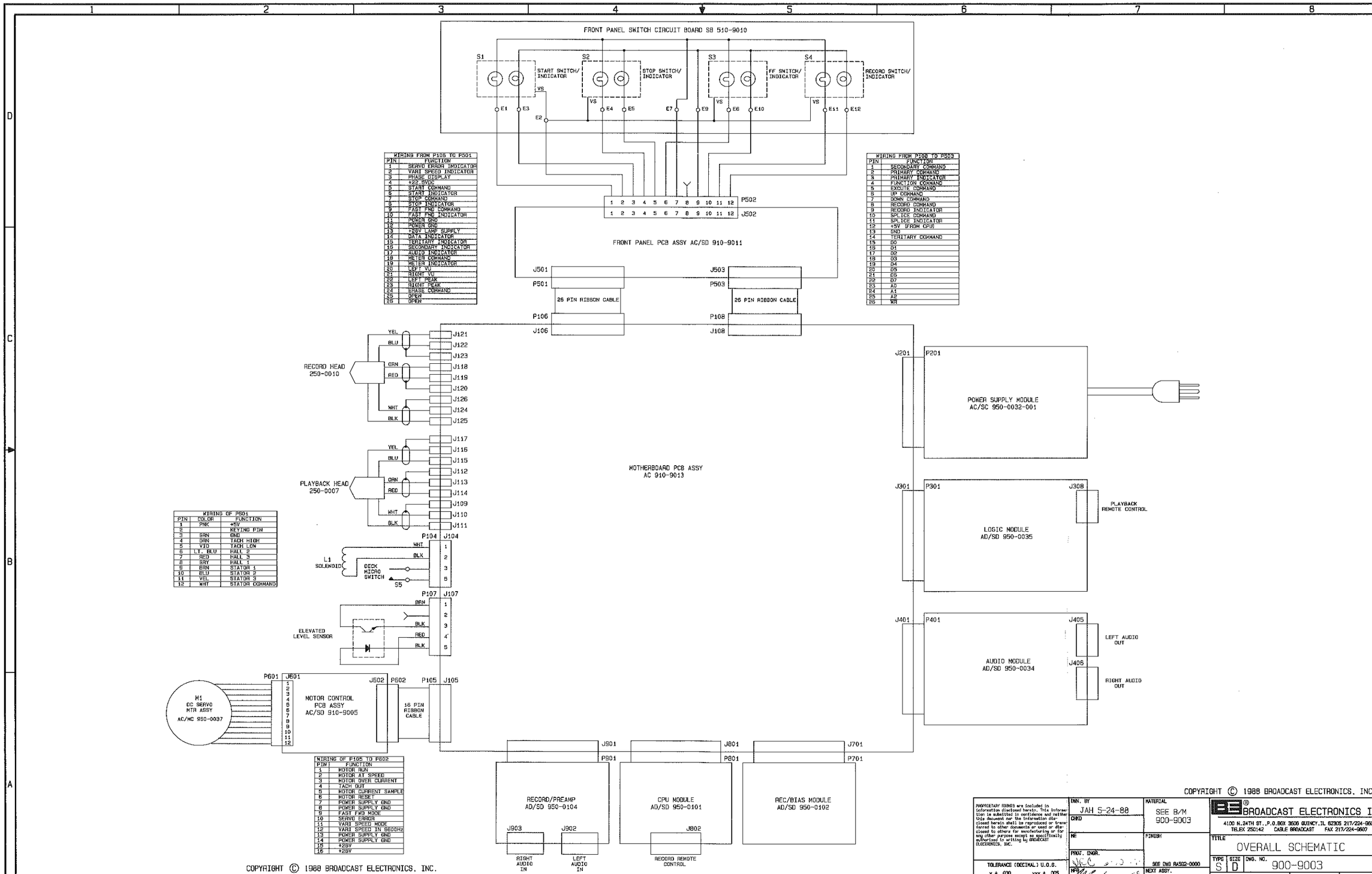
DWN. BY TLL 7-8-87
CHKD
ME
PROJ. ENGR.
MFG.
MATERIAL
FINISH
SEE DWG RA582-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PT-90 OVERALL SCHEMATIC

TYPE	SIZE	DWG. NO.		REV
S	D	900-9000-000 900-9000-300	900-9002-000 900-9000-300	A

MODEL PT-90 PB SCALE NONE SHEET 1 OF 1



TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 5-24-88
CHKD
ENG
PROJ. ENGR.
MFR 6-10-88

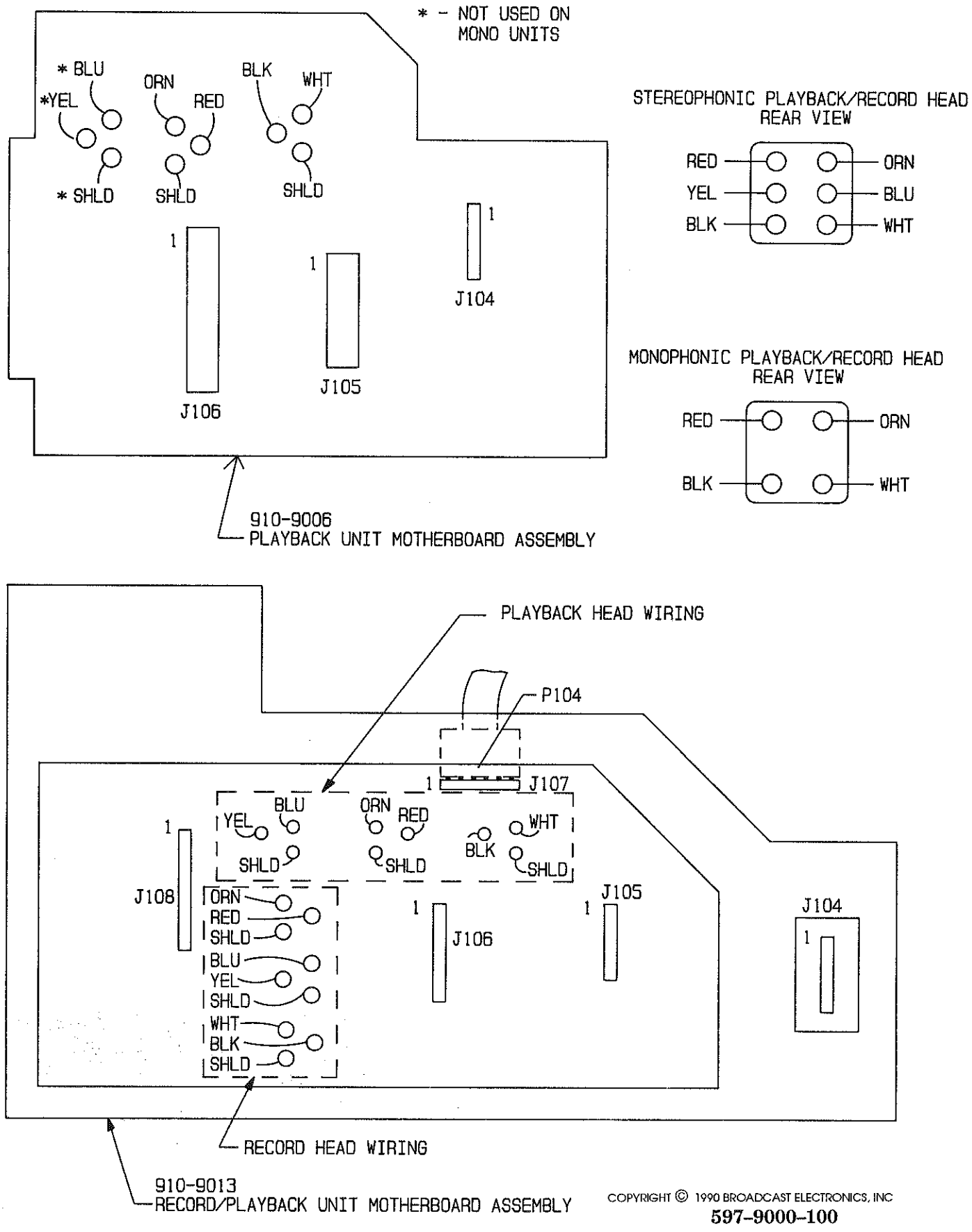
MATERIAL SEE B/M 900-9003
FINISH SEE DWG RASSZ-0000
NEXT ASSY. 950-9001

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE OVERALL SCHEMATIC

TYPE S SIZE D DWG. NO. 900-9003 REV A

MODEL PT-90 RPS SCALE NONE SHEET 1 OF 1



597-9000-100

FIGURE 7-3. 9000 SERIES HEAD TO MOTHERBOARD WIRING DIAGRAM

DETAIL 'C'

LIGHTLY LUBRICATE THREADS OF 'PEM' NUTS WITH SILICONE GREASE (B.E. 700-0137)

409-0020, 2.5" LG.

520-0025, REF.

420-4505, APPLY LOCTITE #242 (B.E. 700-0015) TO MALE THREADS.

430-0010

445-0008

420-4503, 3 PLCS

.068±.010

DIM. AFTER ASSEMBLY

459-0123

430-0011, 2 PLCS

520-0025, MT TO 474-0299 AND 474-0292 WITH (6) 420-6605, SEE DETAIL 'C'

478-0072, MT. TO 474-0299 WITH (2) 420-6605

450-0025 (BLACK)

450-0005 (BLACK)

950-0035

950-0032-001

474-0299, LEFT SIDE PLATE. 474-0292, RIGHT SIDE PLATE (NOT SHOWN FOR CLARITY)

(2) 420-6605

910-9006 MT. TO 520-0026 WITH (6) 420-6106 (6) 423-6002

P107 OF 950-0306

910-9005 MT. TO 474-0299 WITH (3) 420-6605, TIGHTEN 9±1 IN. LBS

409-0002, MT. WITH 700-0148 CUT .25 LG. ONE AT EACH END AS SHOWN, TYP. 4 PLCS

J108

J107

J106

J105

J104

J602

LIGHTLY LUBRICATE THREADS OF 'PEM' NUTS WITH SILICONE GREASE (B.E. 700-0137)

471-0556-001 MT. TO 474-0299 AND 474-0292 WITH (4) 420-6605, SEE SHT. 2 FOR ASSY OF FRONT PANEL.

471-0567

CONNECTS TO J501 ON 910-9003

TRIM LEGS ON 409-0002 FLUSH WITH BOTTOM OF 520-0026 AS SHOWN, 8 PLCS

520-0026 MT. TO 474-0299 AND 474-0292 WITH (9) 420-6605

471-0555 MT. TO 474-0299 AND 474-0292 WITH (4) 420-6605.

403-2194, MT. TO 471-0555 WITH (1) 420-6106, (1) 423-6011, 4 PLCS.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MSE 3-3-87
CHKD
ENG.
PROJ. ENGR. 4-30-87
MFG.

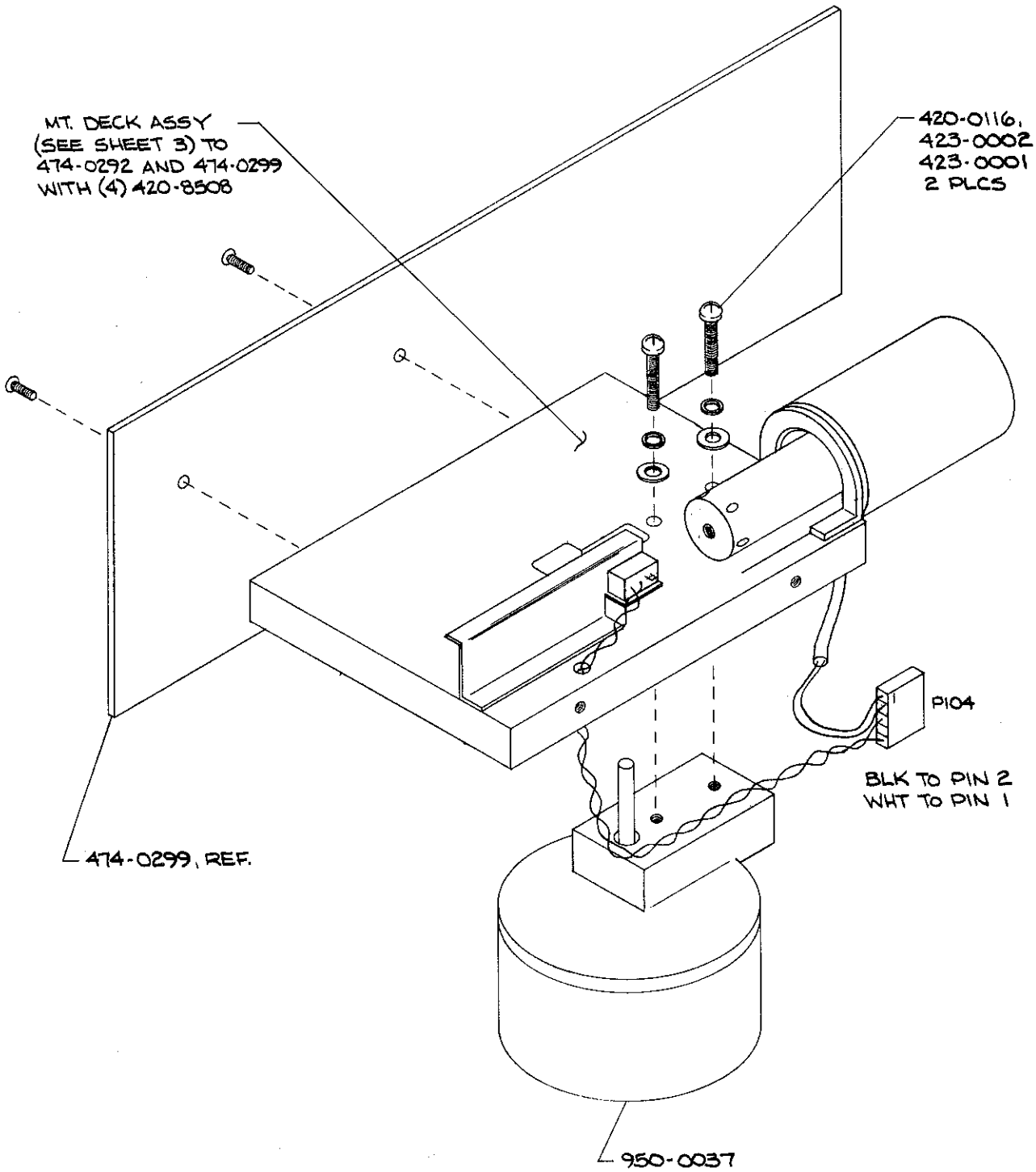
MATERIAL SEE B/M 950-9000
FINISH
SEE DWG RA552-0080
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE ASSY, BASIC 9000 PLAYBACK

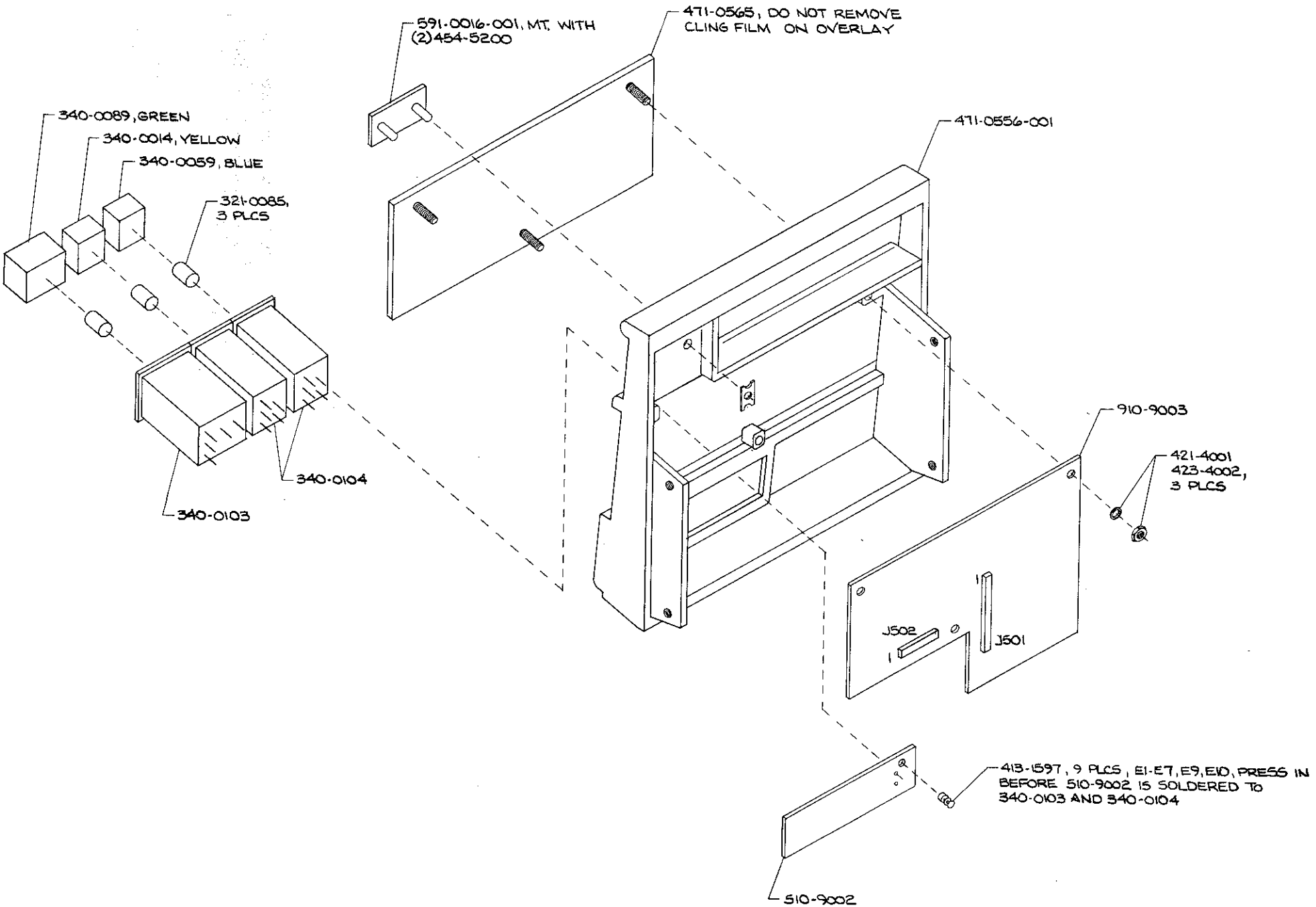
TYPE A | SIZE D | DWG. NO. 950-9000 | REV E

MODEL 9000 | SCALE ~ | SHEET 1 OF 3



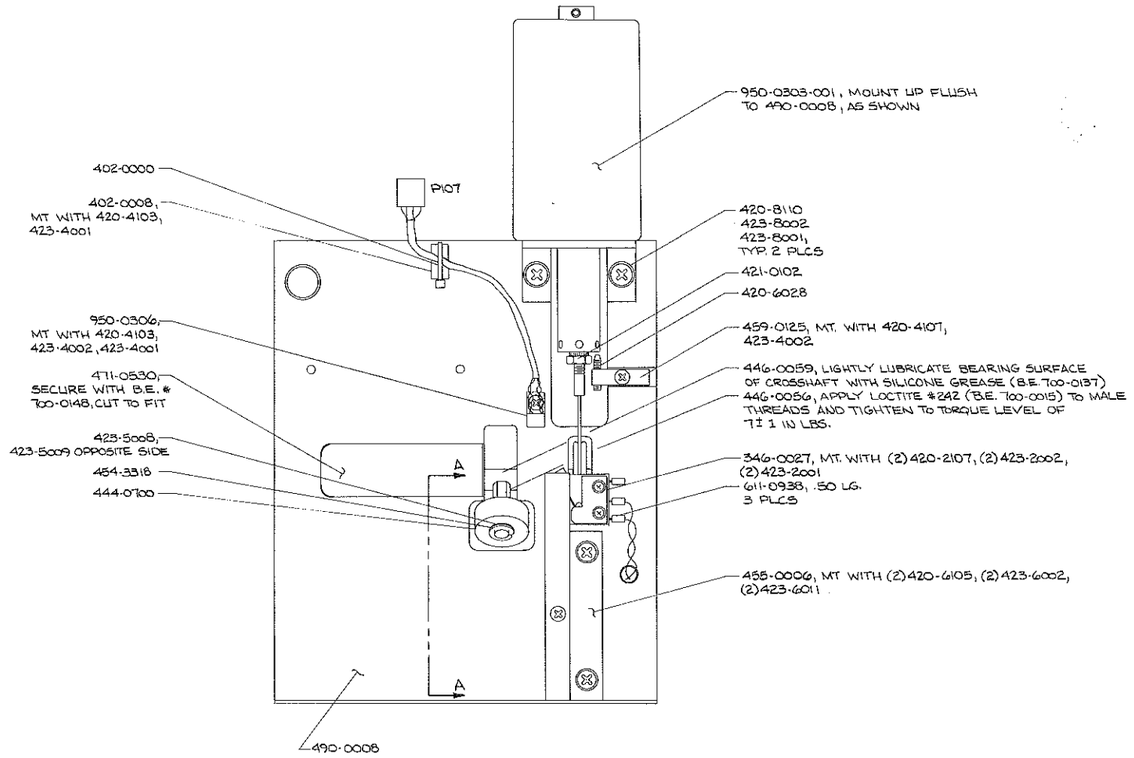
597-9000-120A

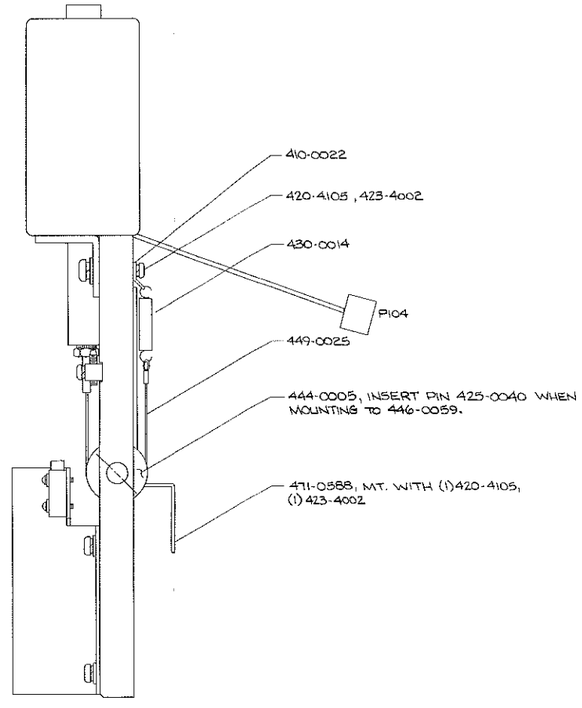
FIGURE 7–4. ASSEMBLY, BASIC 9000 PLAYBACK (AD950–9000)

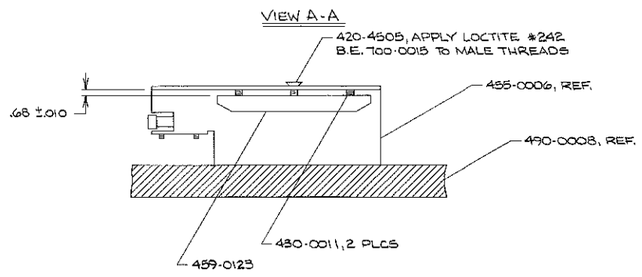


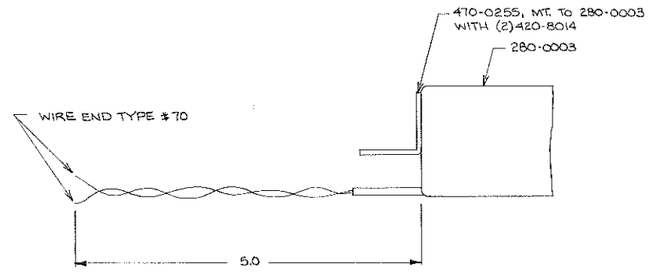
597-9000-120B

FIGURE 7–4. ASSEMBLY, BASIC 9000 PLAYBACK (AD950–9000)









SOLENOID ASSEMBLY #950-0303-001

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MSE 3-3-87
CHKD
ME
PROJ. ENGR. 5-1-87
MFG 5-5-87

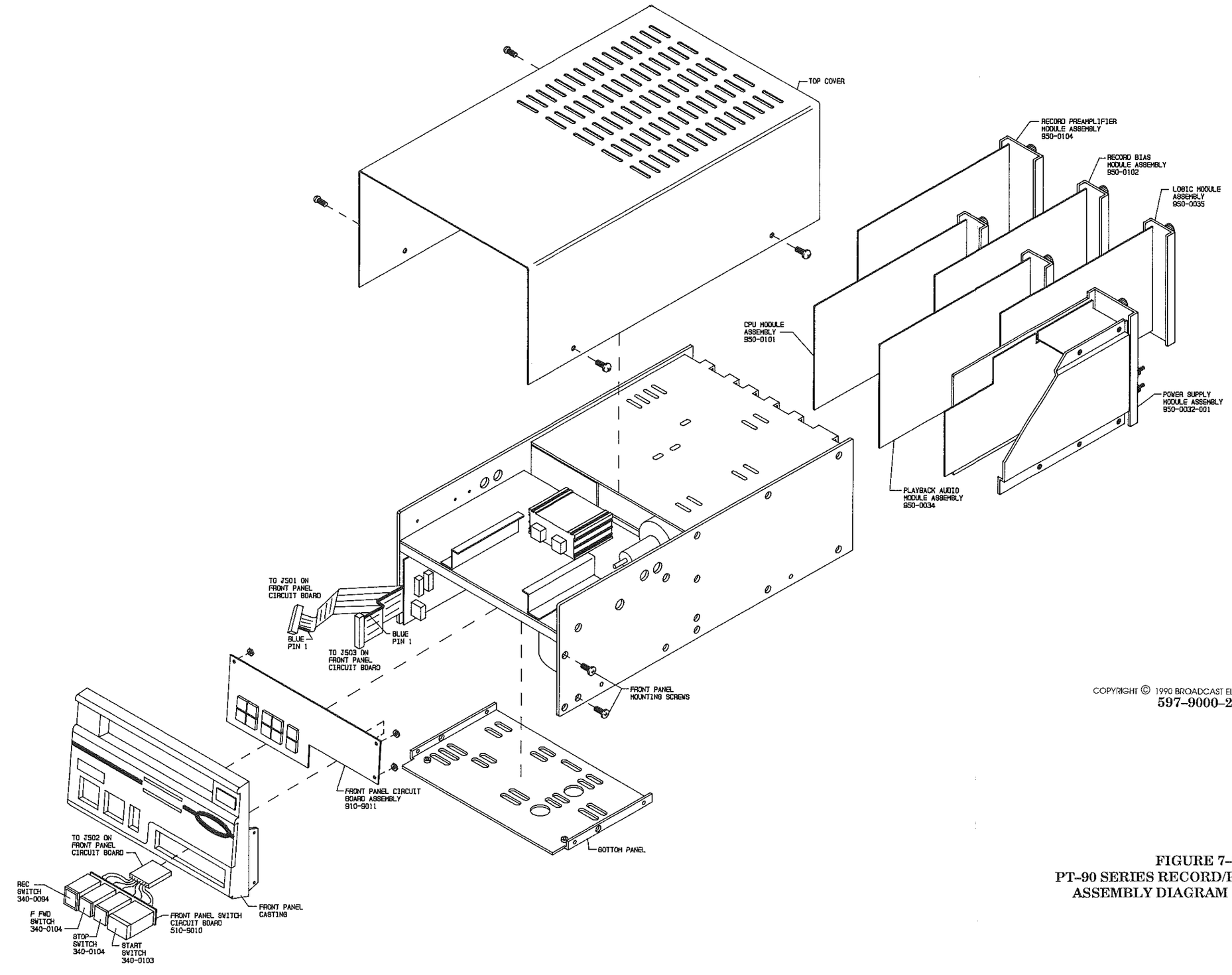
MATERIAL SEE B/M 950-9000
FINISH
SEE DWG RA592-0000 NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE ASSY, BASIC 9000 PLAYBACK

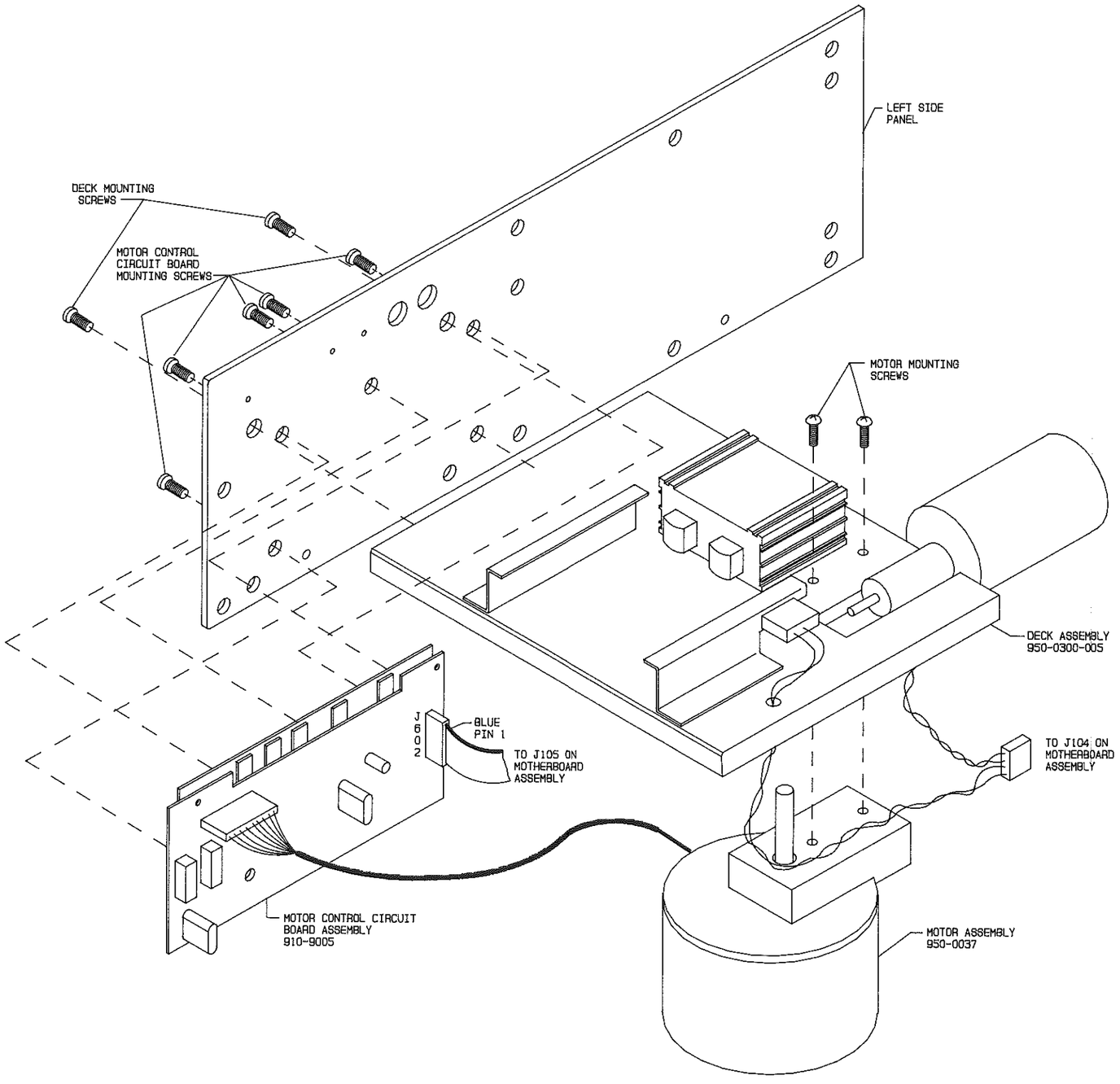
TYPE	SIZE	DWG. NO.	REV
A	D	950-9000	E

MODEL 9000 SCALE ~ SHEET 3 OF 3



597-9000-200

FIGURE 7-5.
PT-90 SERIES RECORD/PLAYBACK UNIT ASSEMBLY DIAGRAM (Sheet 1 of 4)



597-9000-200

FIGURE 7–5.
PT–90 SERIES RECORD/PLAYBACK UNIT ASSEMBLY DIAGRAM (Sheet 2 of 4)

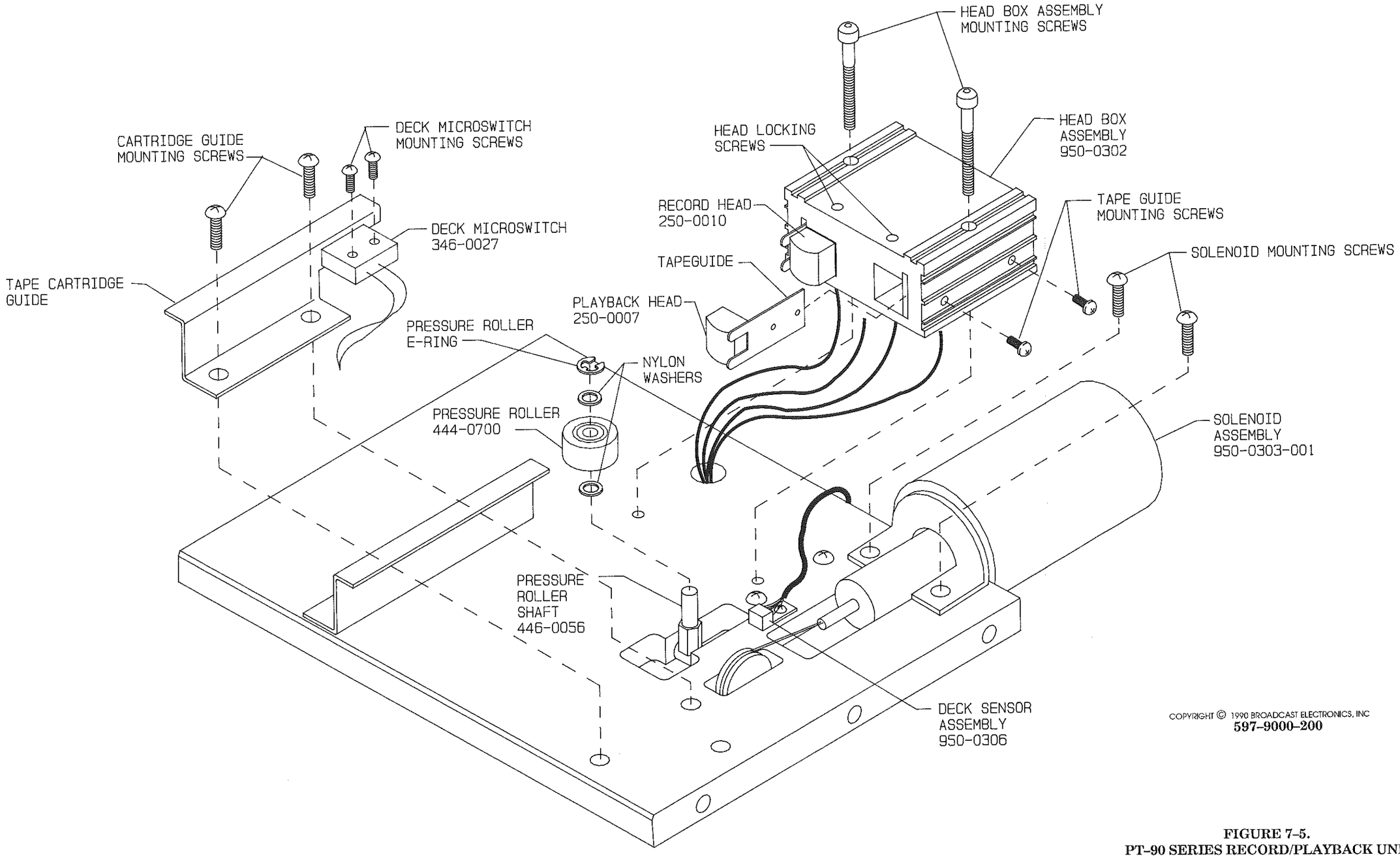
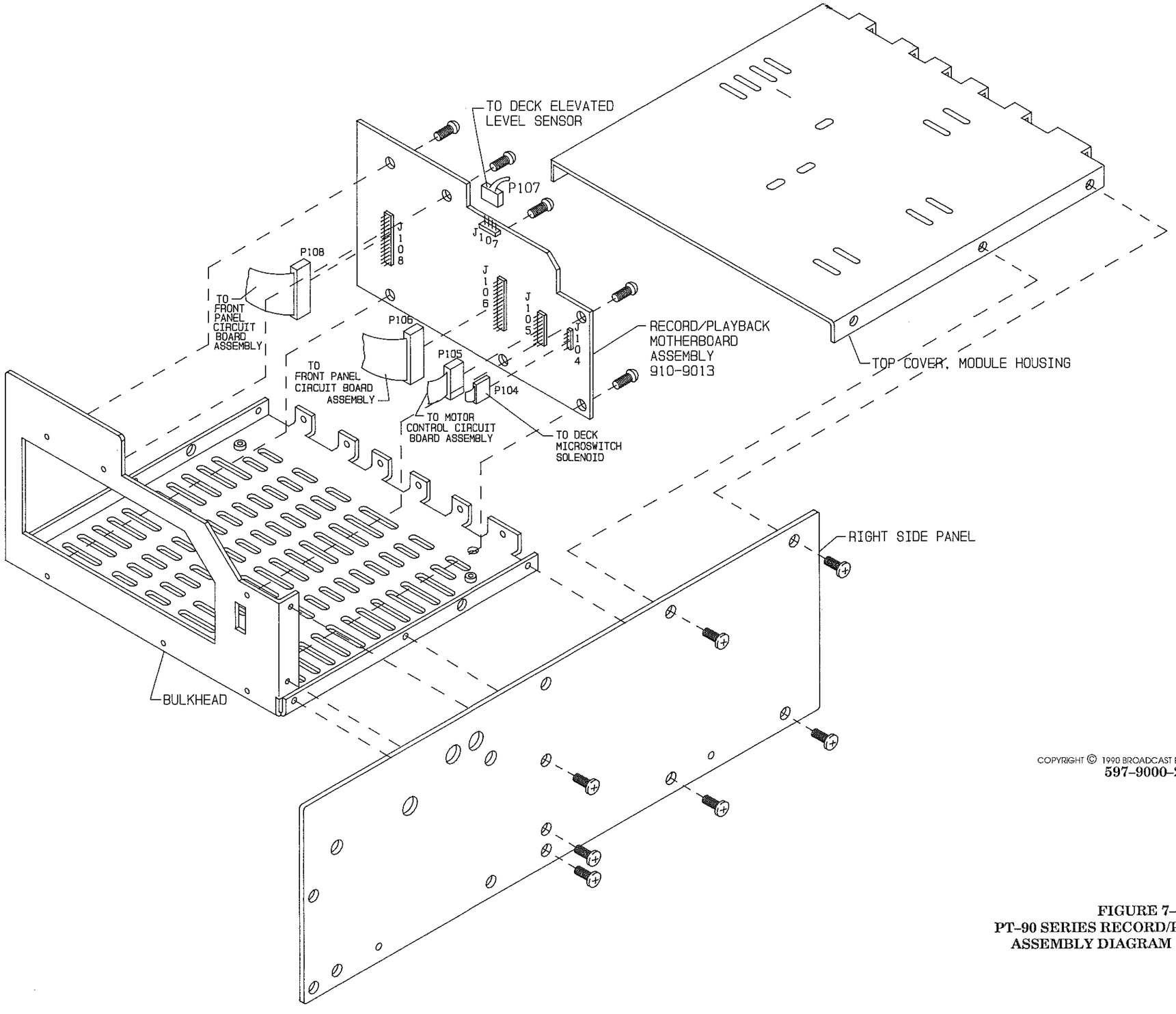
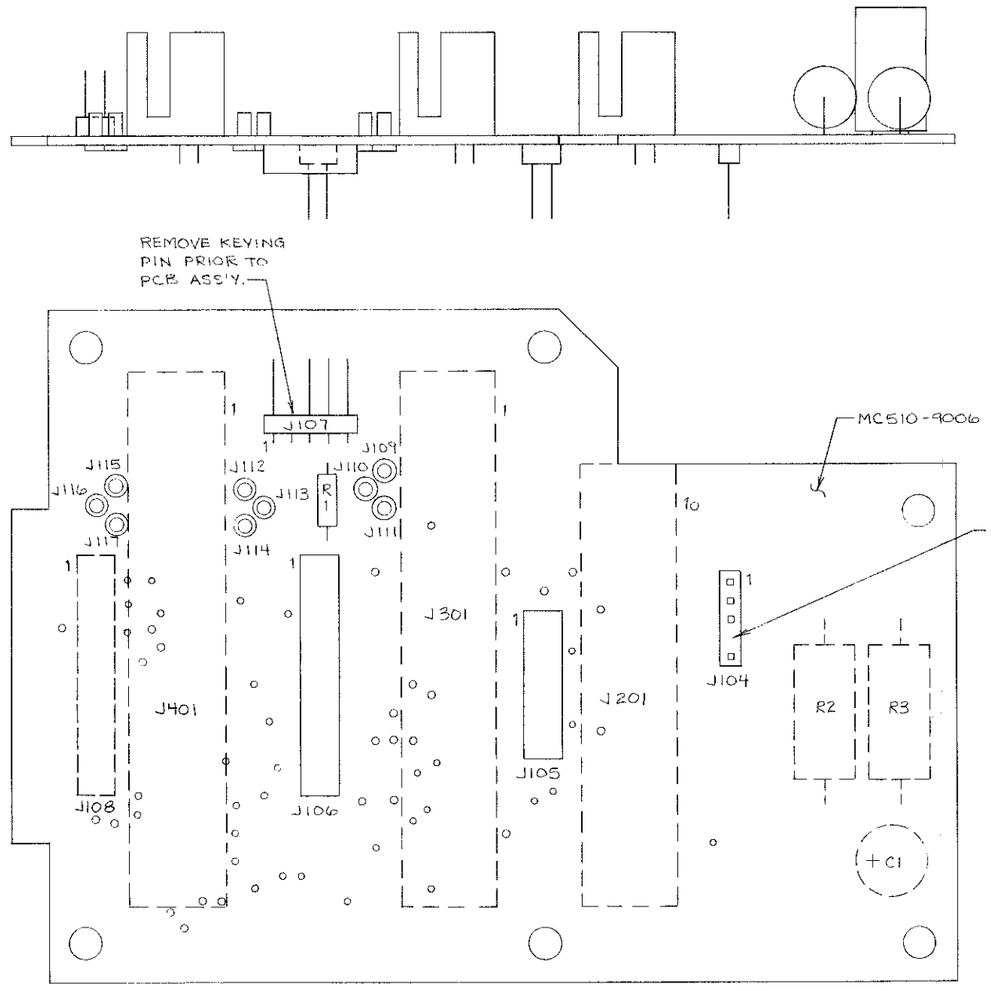


FIGURE 7-5.
PT-90 SERIES RECORD/PLAYBACK UNIT ASSEMBLY DIAGRAM (Sheet 3 of 4)



597-9000-200

FIGURE 7-5.
PT-90 SERIES RECORD/PLAYBACK UNIT ASSEMBLY DIAGRAM (Sheet 4 of 4)



NOTES:

1. AFTER COMPONENTS ON COMPONENT SIDE OF BOARD ARE WAVE SOLDERED, THEN J201, J301, & J401 ARE TO BE INSTALLED USING APPROPRIATE SEATING TOOLS AS PER AMP APPLICATION SPECIFICATION NO. 114-9009 REV C SHEET 1 THRU 8 DATED 3-6-86

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY KLS 11-4-86
CHKD MH 5-5-87
ME 5-5-87
PROJ. ENGR. 4-7-87 JRC
MFG. MC 5-4-87

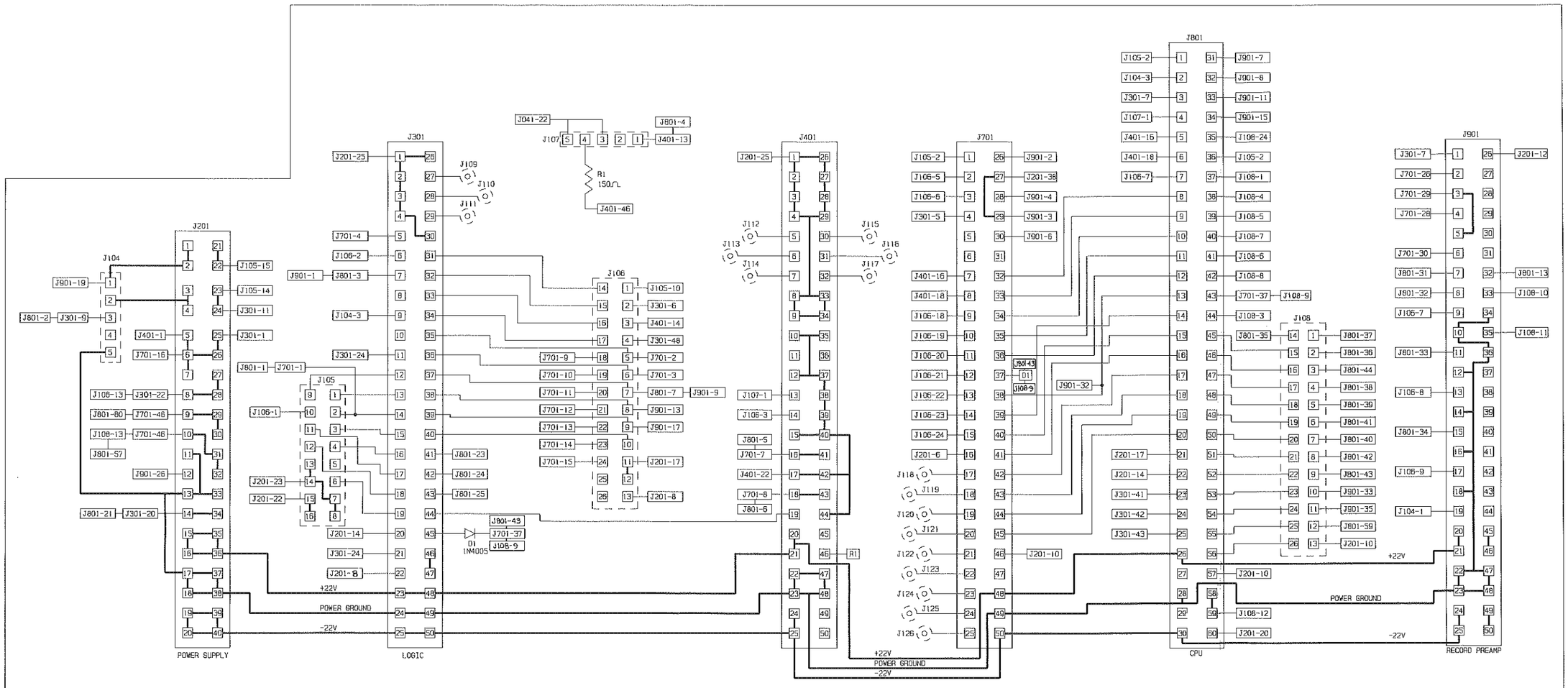
MATERIAL SEE B/M 910-9006
FINISH
~~SEE DWG RA592-8000~~
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY — MOTHER BD.

TYPE	SIZE	DWG. NO.	REV
A	C	910-9006	B

MODEL PT90 PB SCALE 2/1 SHEET 1 OF 1



TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

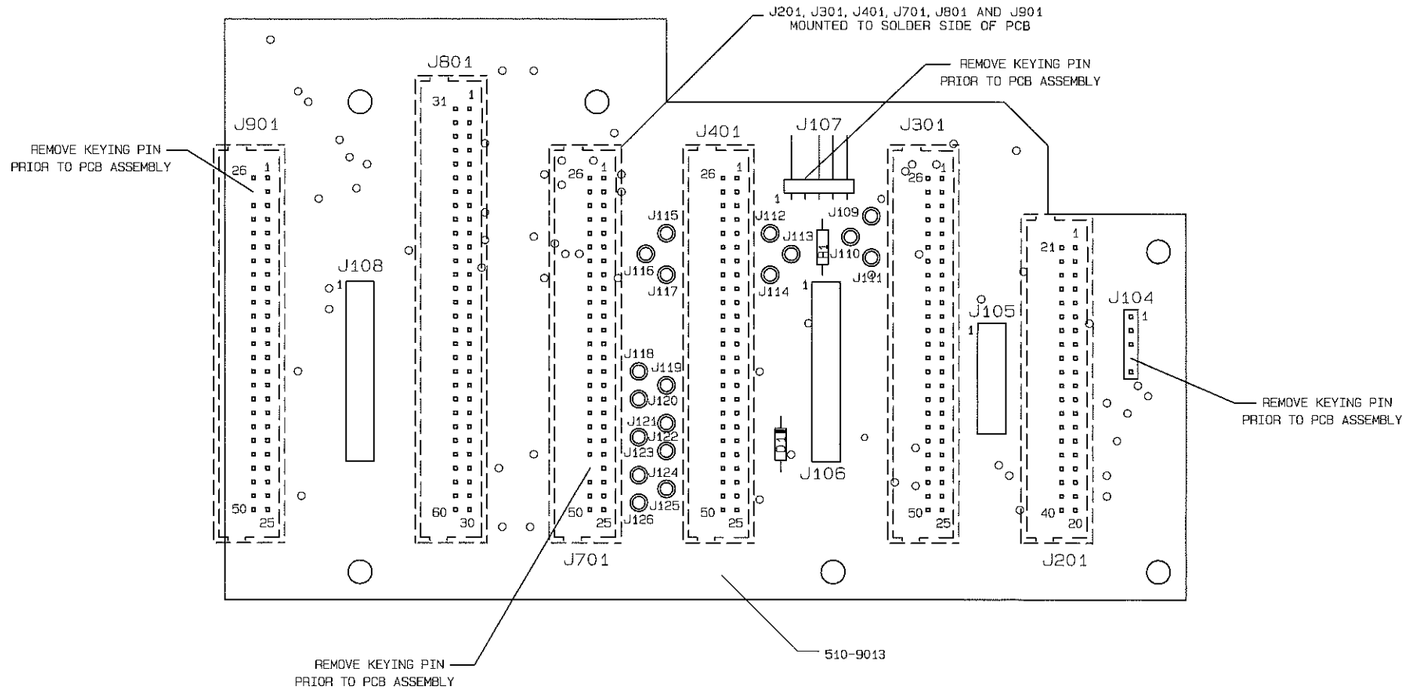
DWN. BY TLL 8-12-88
CHKD
ENGR
PROJ. ENGR.
MFG.
MATERIAL
FINISH
SEE DWG RA592-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE
PT-90 RPS MOTHERBOARD SCHEMATIC

TYPE S | SIZE D | DWG. NO. 910-9013 | REV C

MODEL PT-90 | SCALE NONE | SHEET 1 OF 1



NOTE:

1. AFTER COMPONENTS ON COMPONENT SIDE OF BOARD ARE WAVE SOLDERED, THEN INSTALL J201, J301, J401, J701, J801 AND J901. THEY ARE TO BE INSTALLED USING APPROPRIATE SEATING TOOLS, AS PER AMP APPLICATION SPECIFICATION NO. 114-9009 REV O SHEET 1 THRU 8.

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN BY MERK 12-8-87
CHKD
ME
PROJ. ENGR.
MFG.

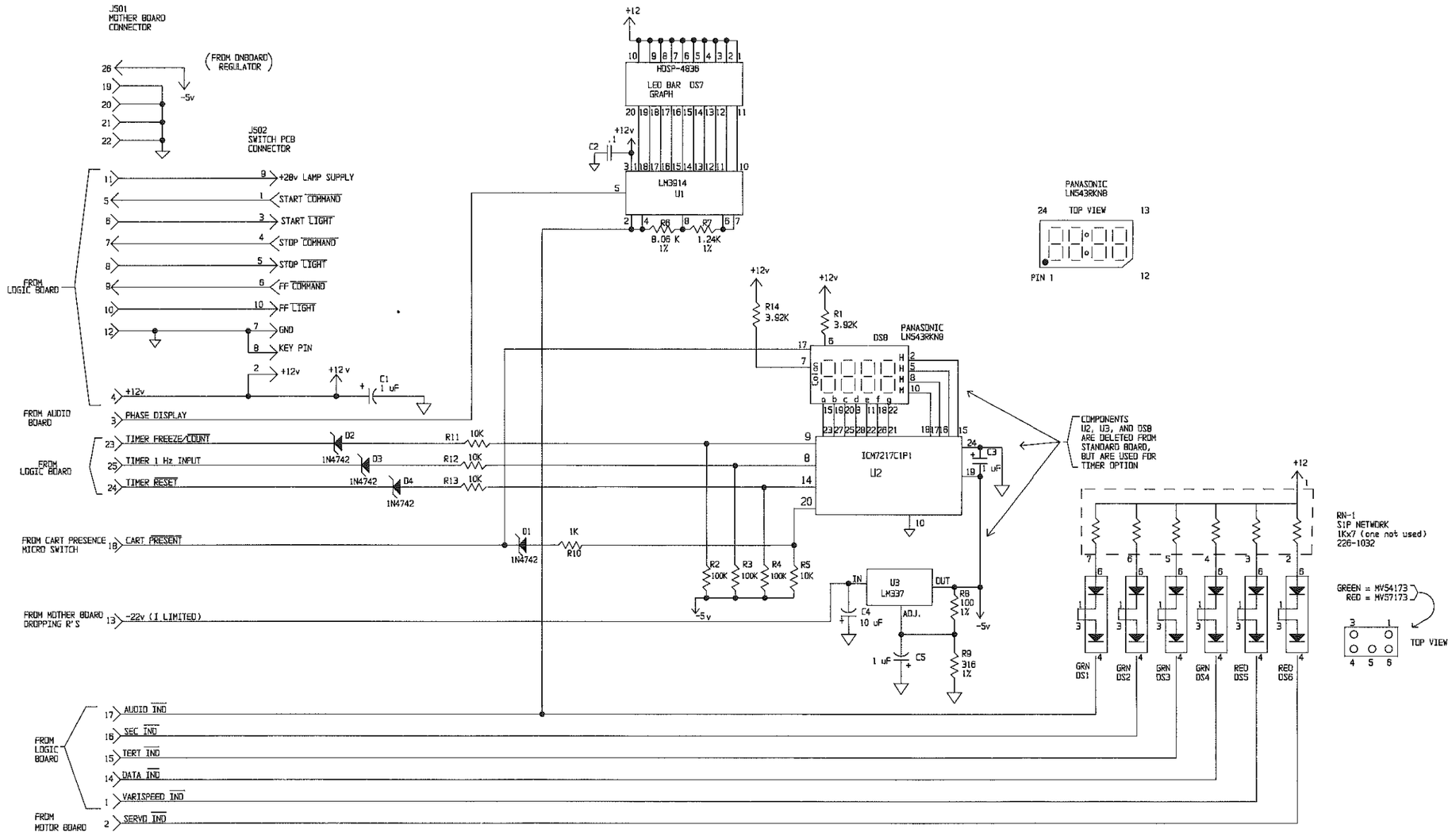
MATERIAL SEE B/M 910-9013
FINISH
NEXT ASSY 950-9001

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250143 CABLE BROADCAST FAX 217/224-9607

TITLE PCB ASSEMBLY-MOTHERBOARD

TYPE	SIZE	DWG.NO.	REV
A	D	910-9013	A

MODEL PT90 RPS SCALE 2/1 SHEET 1 OF 1



TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY 8-12-92
M. HAYDEN
CHKD
ENGR
PROJ. ENGR.
MFG.

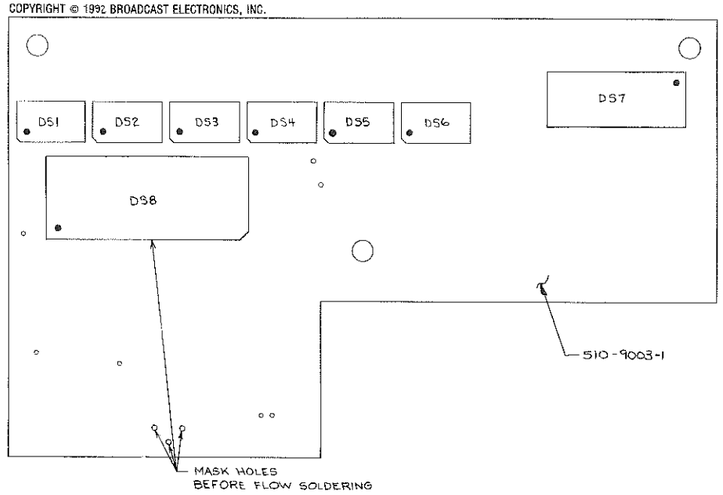
MATERIAL
FINISH
SEE DWG RA582-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3806 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

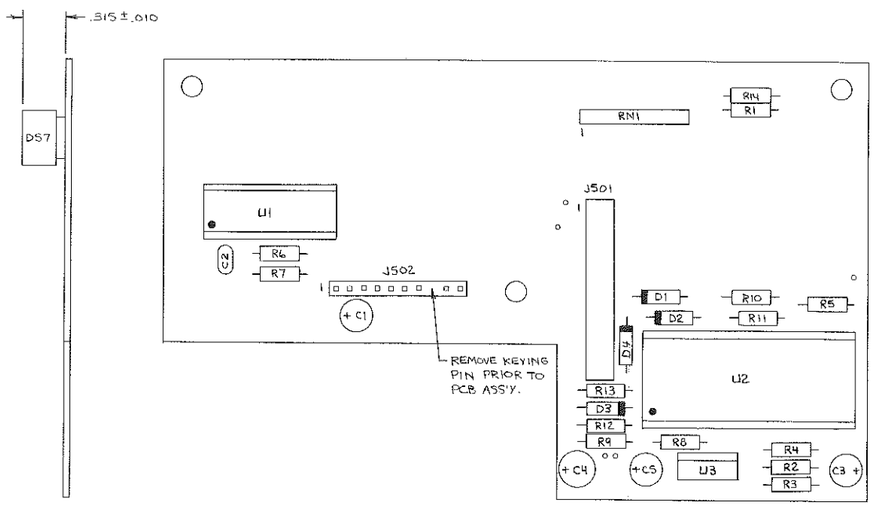
TITLE
SCHEMATIC FRONT PANEL
STATUS BOARD PT90PS

TYPE	SIZE	DWG. NO.	REV
S	C	910-9003-1	A

MODEL | SCALE NONE | SHEET 1 OF 1



SOLDER SIDE



COMPONENT SIDE

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY Archives 8-8-92
CHKD MH 8-11-92
ME
PROJ. ENGR. 8-11-92
MFG.

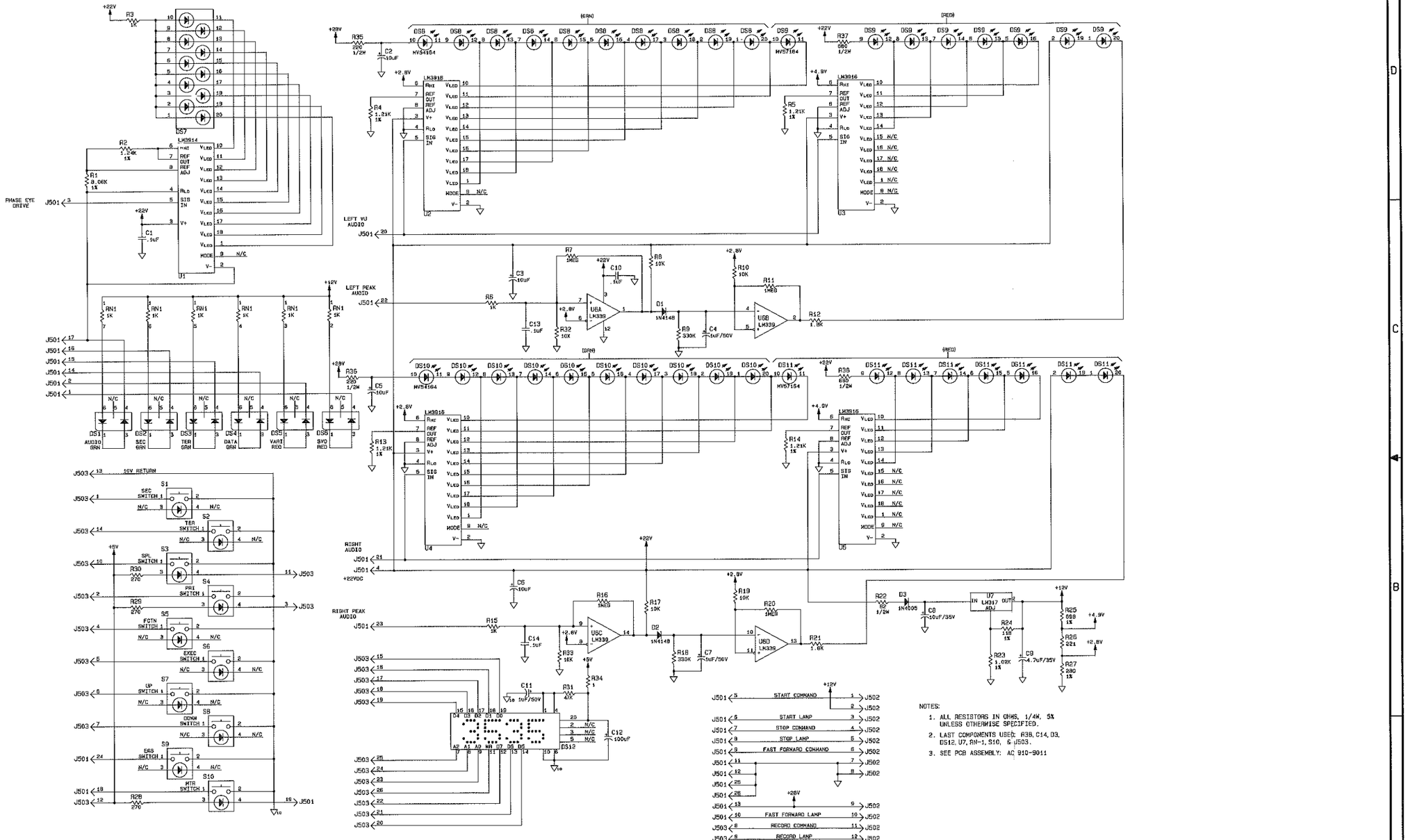
MATERIAL SEE B/M 910-9003-1
FINISH
~~SEE DWG 9A592-0000~~
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3506 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY — FRONT PANEL BD.

TYPE A | SIZE D | DWG. NO. 910-9003-1 | REV 4

MODEL PT90 PB | SCALE 2/1 | SHEET 1 OF 1



NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: R38, C14, D9, DS12, U7, RN-1, S10, & J503.
3. SEE PCB ASSEMBLY: AC 910-9011

DWN. BY	JAH 11-4-87
CHKD	
ME	
PROJ. ENGR.	
MFG	
MATERIAL	SEE B/M 950-0102
FINISH	SEE DWG RA502-0000
NEXT ASSY.	950-9001

TOLERANCE (DECIMAL) U.O.S. .xx ± .030 .xxx ± .005 .xx ± .015 ANGLES ± 1°

BROADCAST ELECTRONICS INC.
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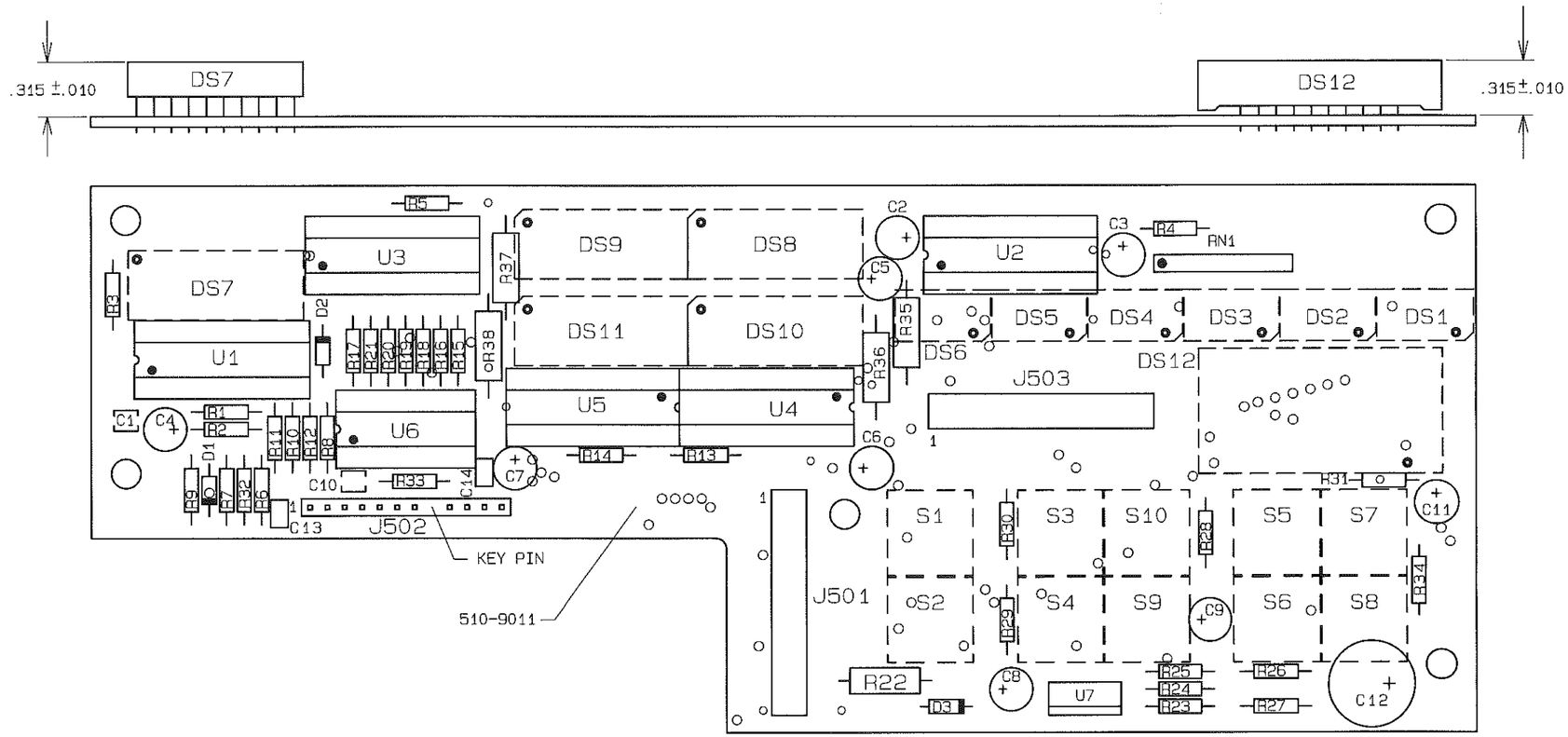
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE: FRONT PANEL STATUS

TYPE	SIZE	DWG. NO.	REV
S	D	910-9011	A

MODEL PT-90 P/S | SCALE NONE | SHEET 1 OF 1



NOTE:

1. SEE SCHEMATIC SD910-9011
2. CUT PIN 8 OF J502.

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN BY MERK 6-17-87
CHKD
ME 6-10-87
PROJ. ENGR.
MFG 6-10-87

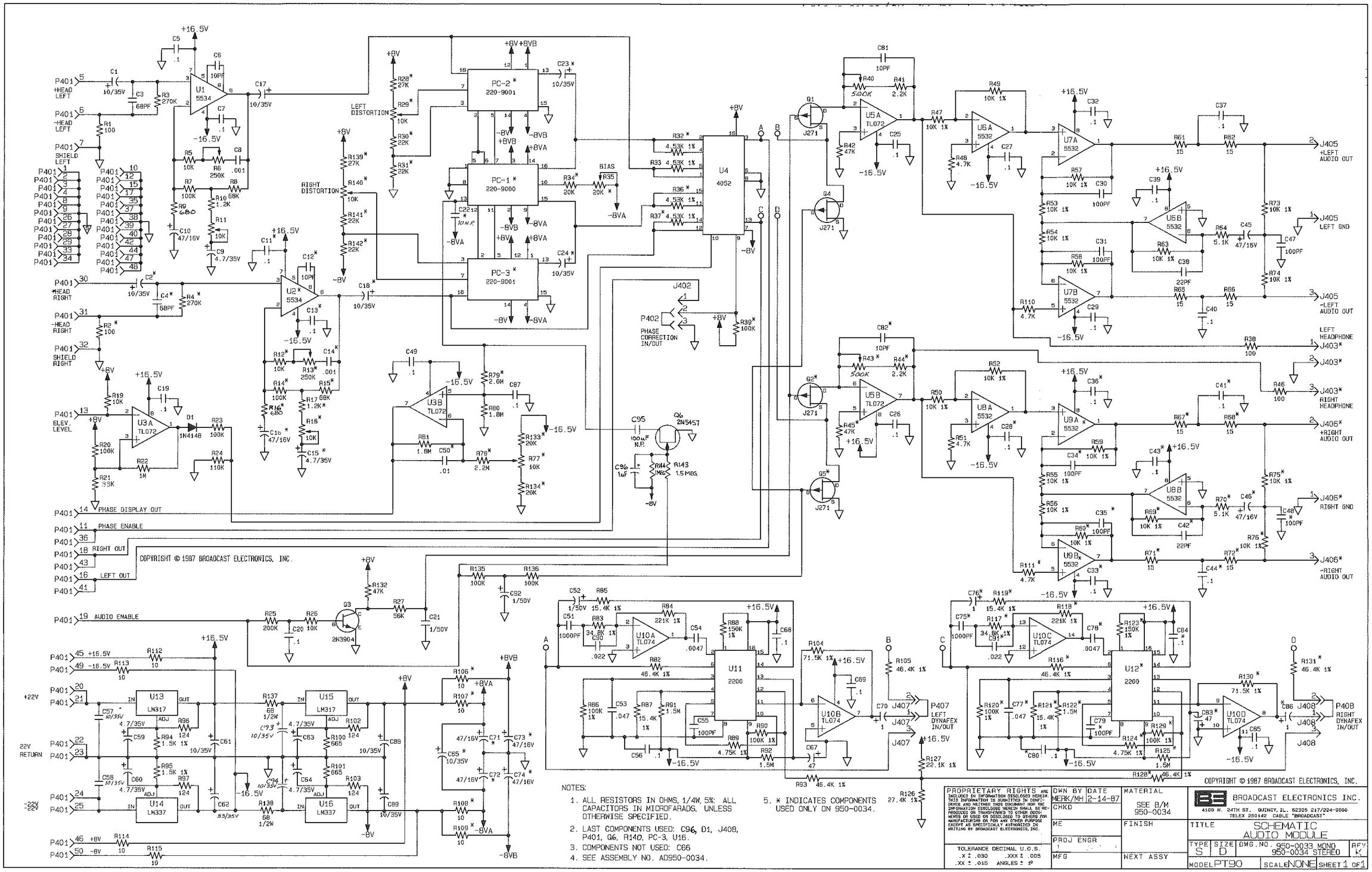
MATERIAL SEE B/M 910-9011
FINISH
NEXT ASSY 950-9001

BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/324-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE PCB ASSEMBLY- FRONT PANEL STATUS

TYPE	SIZE	DWG.NO.	REV
A	C	910-9011	B

MODEL PT90RPS SCALE 2/1 SHEET 1 OF 1



NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5%: ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: C96, D1, J408, P401, Q6, R140, PC-3, U16.
3. COMPONENTS NOT USED: C66
4. SEE ASSEMBLY NO. AD950-0034.
5. * INDICATES COMPONENTS USED ONLY ON 950-0034.

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

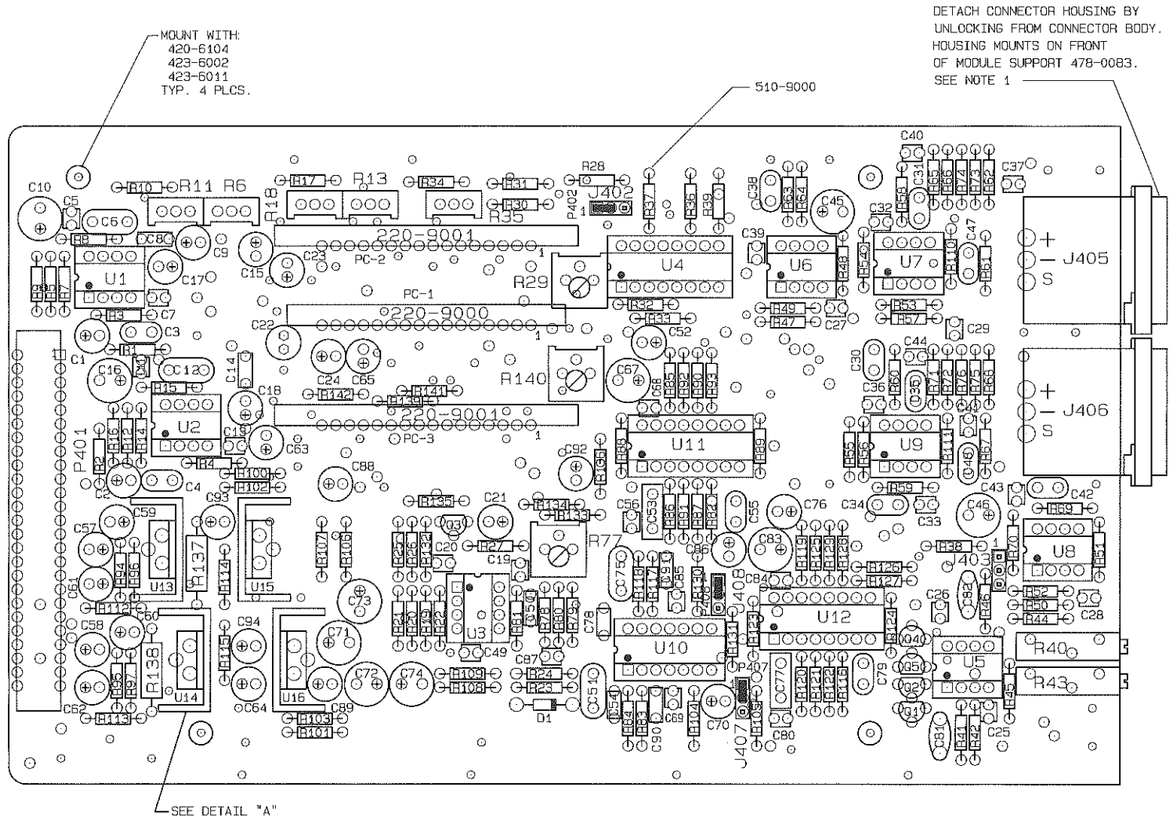
DWN BY	DATE	MATERIAL
MERK/MH	2-14-87	SEE B/M 950-0034
CHKD		
ME		FINISH
PROJ ENGR		
MFG		NEXT ASSY

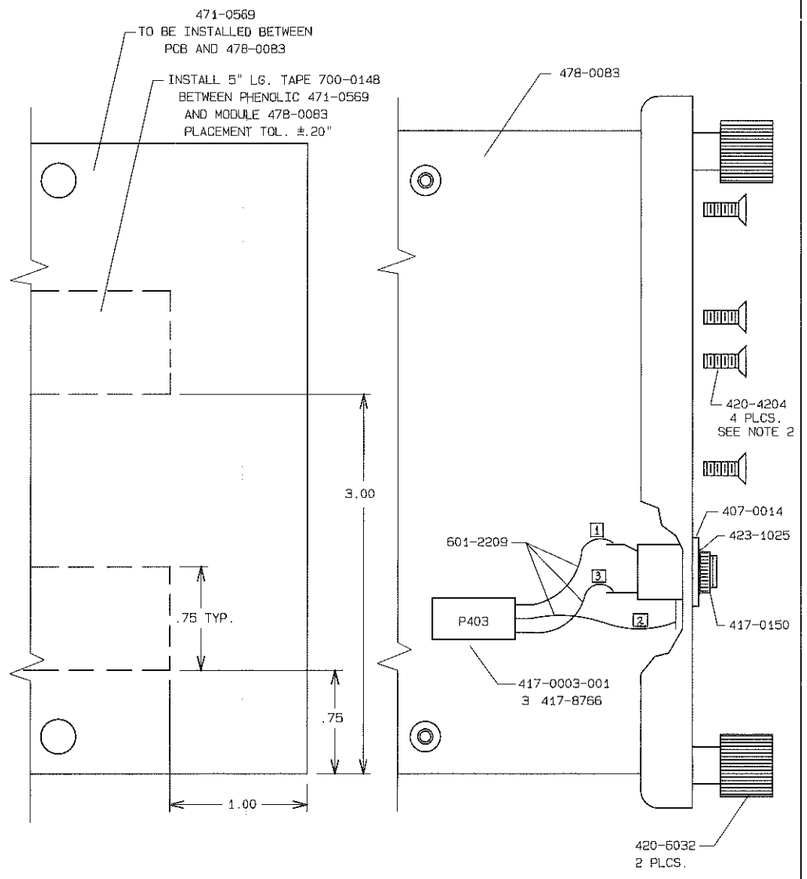
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST. QUINCY, IL. 62305 217/224-9600
TELEX 250142 CABLE "BROADCAST"

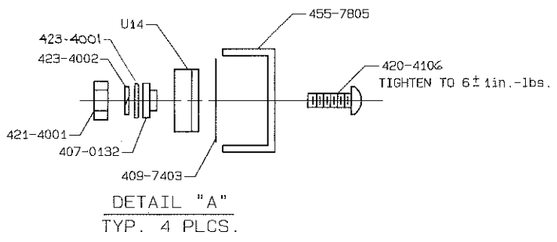
TITLE SCHEMATIC AUDIO MODULE

TYPE	SIZE	DWG. NO.	REV
S	D	950-0033 MONO 950-0034 STEREO	K

MODEL PT90 SCALE NONE SHEET 1 OF 1







DETAIL "A"
TYP. 4 PLCS.

NOTES:

1. MOUNT J405 AND J406 TO 478-0083 BEFORE SOLDERING TO PCB.
2. APPLY LOCKTITE 242 700-0015 TO 420-4204, 4 PLCS.
3. TEST PCB BEFORE ADDING MODULE SUPPORT 478-0083.
4. TRIM ALL COMPONENT LEADS TO .040 ± .010.
5. COMPONENTS USED ON 950-0034 ONLY: R2, R4, R12-R18, R28-R32, R34-R37, R39, R43-R46, R50-R52, R55, R56, R59-R60, R67-R72, R75-R79, R106-R109, R111, R116-R125, R128-R131, R133, R134, R139-R142, C2, C4, C11-C16, C18, C22-C24, C28, C33-C36, C41-C44, C46, C48, C50, C65, C71-C80, C82-C84, C86, C91, Q2, Q5, U2, U8, U9, U12, XU2, XU8, XU9, XU12, PC1-PC3, J408, P408, J406.

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TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

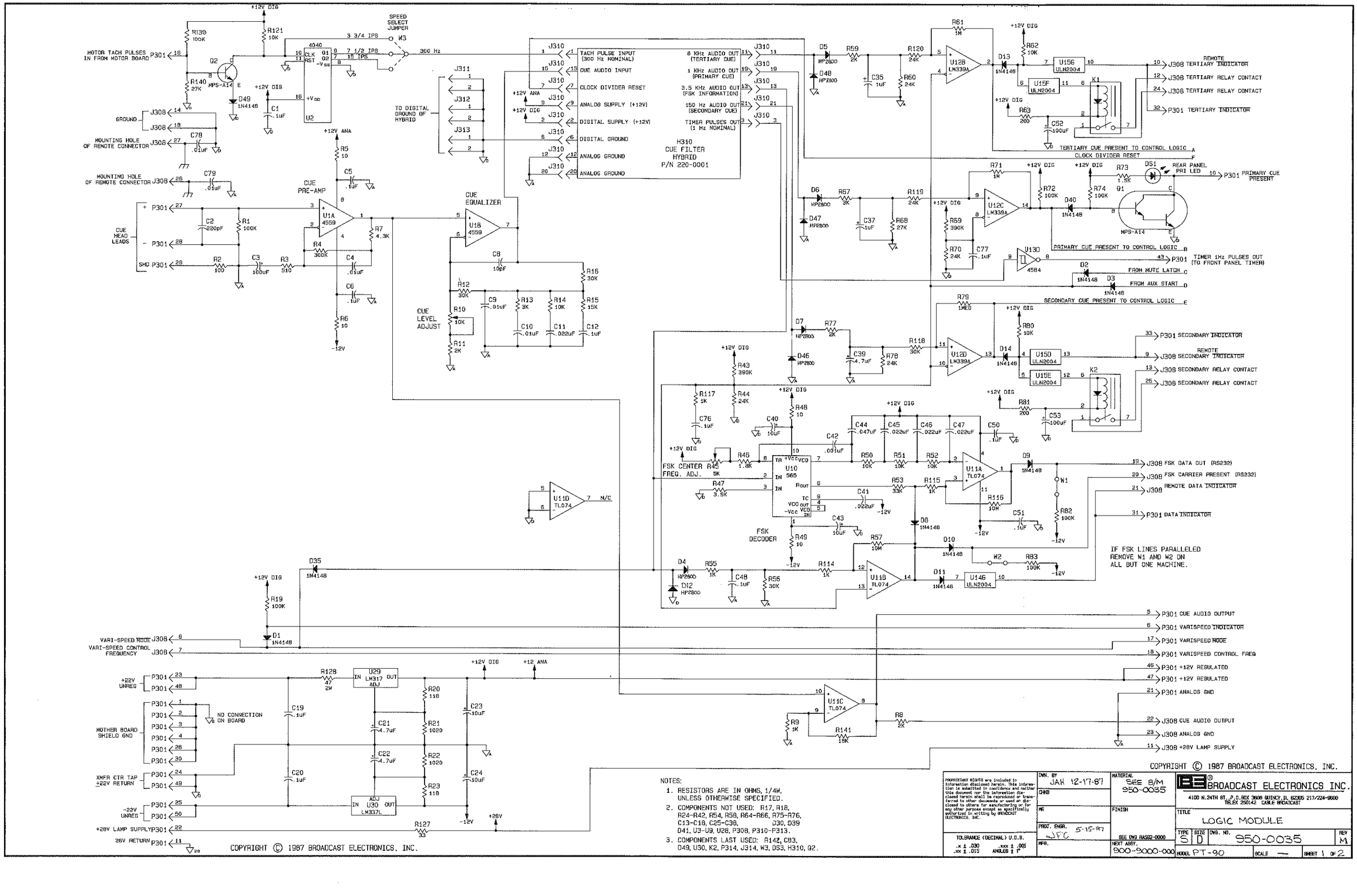
DWN BY	MERK 1-27-87
CHKD	
ME	5-15-87 JH STEINKAMP
PROJ. ENGR.	JRC 5-15-87
MFG.	5-15-87 PR BROSE
MATERIAL	SEE B/M 950-0033/34
FINISH	
NEXT ASSY	

BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE: AUDIO MODULE ASSEMBLY

TYPE	SIZE	DWG.NO.	REV
A	D	950-0033/34	K

MODEL PT90 SCALE 2/1 SHEET 1 OF 1


MOTOR TACH PULSES IN FROM MOTOR BOARD P301 16
GROUND J308 14
J308 18
MOUNTING HOLE OF REMOTE CONNECTOR J308 27
MOUNTING HOLE OF REMOTE CONNECTOR J308 26
CUE HEAD LEADS
P301 27
P301 28
SHD P301 29
+12V DIG
SPEED SELECT JUMPER
3 3/4 IPS
7 1/2 IPS
15 IPS
300 Hz
TO DIGITAL GROUND OF HYBRID
+12V ANA
-12V
CUE PRE-AMP
CUE EQUALIZER
CUE LEVEL ADJUST
TACH PULSE INPUT (300 Hz NOMINAL)
CUE AUDIO INPUT
CLOCK DIVIDER RESET
ANALOG SUPPLY (+12V)
DIGITAL SUPPLY (+12V)
DIGITAL GROUND
ANALOG GROUND
ANALOG GROUND
8 KHz AUDIO OUT (TERTIARY CUE)
1 KHz AUDIO OUT (PRIMARY CUE)
3.5 KHz AUDIO OUT (FSK INFORMATION)
150 Hz AUDIO OUT (SECONDARY CUE)
TIMER PULSES OUT (1 Hz NOMINAL)
H310
CUE FILTER
HYBRID
P/N 220-0001
REMOTE TERTIARY INDICATOR
J308 TERTIARY RELAY CONTACT
J308 TERTIARY RELAY CONTACT
P301 TERTIARY INDICATOR
TERTIARY CUE PRESENT TO CONTROL LOGIC
CLOCK DIVIDER RESET
REAR PANEL PRI LED
P301 PRIMARY CUE PRESENT
PRIMARY CUE PRESENT TO CONTROL LOGIC
TIMER 1Hz PULSES OUT (TO FRONT PANEL TIMER)
FROM MUTE LATCH
FROM AUX START
SECONDARY CUE PRESENT TO CONTROL LOGIC
REMOTE SECONDARY INDICATOR
P301 SECONDARY INDICATOR
J308 SECONDARY RELAY CONTACT
J308 SECONDARY RELAY CONTACT
FSK CENTER FREQ. ADJ. R45 5K
FSK DECODER
J308 FSK DATA OUT (RS232)
J308 FSK CARRIER PRESENT (RS232)
J308 REMOTE DATA INDICATOR
P301 DATA INDICATOR
IF FSK LINES PARALLELED REMOVE W1 AND W2 ON ALL BUT ONE MACHINE.
VARI-SPEED MODE J308 6
VARI-SPEED CONTROL FREQUENCY J308 7
+22V UNREG P301 23
P301 48
MOTHER BOARD SHIELD GND
NO CONNECTION ON BOARD
XFMR CTR TAP +22V RETURN P301 24
P301 49
-22V UNREG P301 25
P301 50
+28V LAMP SUPPLY P301 22
28V RETURN P301 11
P301 CUE AUDIO OUTPUT 5
P301 VARISPEED INDICATOR 6
P301 VARISPEED MODE 17
P301 VARISPEED CONTROL FREQ 18
P301 +12V REGULATED 46
P301 +12V REGULATED 47
P301 ANALOG GND 21
J308 CUE AUDIO OUTPUT 22
J308 ANALOG GND 23
J308 +28V LAMP SUPPLY 11
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NOTES:
1. RESISTORS ARE IN OHMS, 1/4W, UNLESS OTHERWISE SPECIFIED.
2. COMPONENTS NOT USED: R17, R18, R24-R42, R54, R58, R64-R66, R75-R76, C13-C18, C25-C36, D30, D39 D41, U3-U9, U28, P308, P310-P313.
3. COMPONENTS LAST USED: R142, C83, D49, U30, K2, P314, J314, W3, DS3, H310, Q2.
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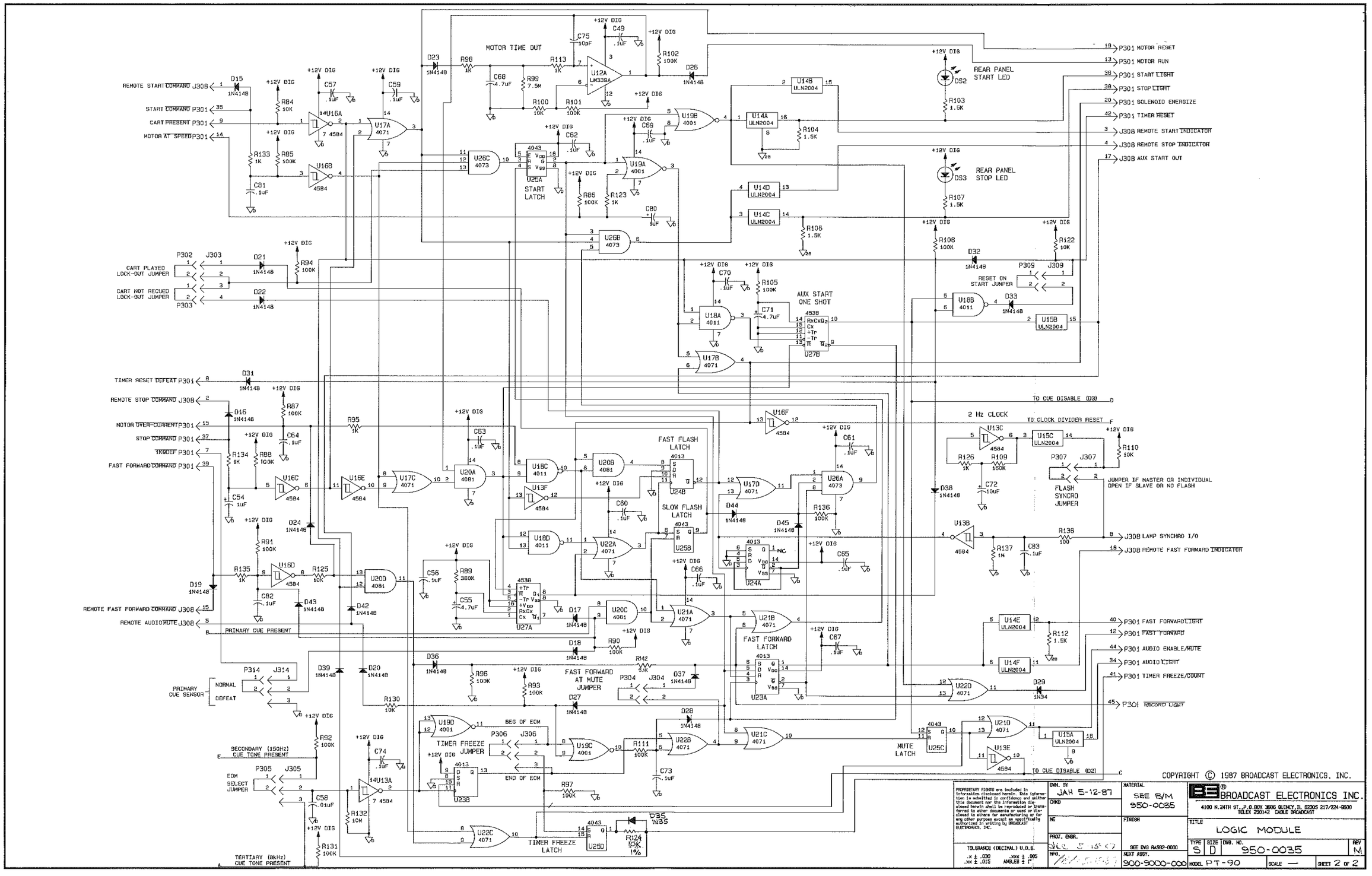
TOLERANCE (DECIMAL) U.O.S. .x ± .030 .xx ± .005 .xxx ± .015 ANGLES ± 1°
DWN. BY JAH 12-17-87
CHKD
ENG
PROJ. ENGR. JFC 5-15-87
MFR.
MATERIAL SEE B/M 950-0035
FINISH
SEE DWG RA382-0000
NEXT ASSY. 900-9000-000
BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600 TELEX 250142 CABLE BROADCAST
TITLE LOGIC MODULE
TYPE SID SIZE D DWG. NO. 950-0035 REV M
MODEL PT-90 SCALE — SHEET 1 OF 2


MOTOR TIME OUT
REMOTE START COMMAND J308
START COMMAND P301
CART PRESENT P301
MOTOR AT SPEED P301
START LATCH
CART PLAYED LOCK-OUT JUMPER
CART NOT RECUED LOCK-OUT JUMPER
AUX START ONE SHOT
REAR PANEL START LED
REAR PANEL STOP LED
RESET ON START JUMPER
P301 MOTOR RESET
P301 MOTOR RUN
P301 START LIGHT
P301 STOP LIGHT
P301 SOLENOID ENERGIZE
P301 TIMER RESET
J308 REMOTE START INDICATOR
J308 REMOTE STOP INDICATOR
J308 AUX START OUT
TIMER RESET DEFEAT P301
REMOTE STOP COMMAND J308
MOTOR OVER-CURRENT P301
STOP COMMAND P301
TKODEF P301
FAST FORWARD COMMAND P301
REMOTE FAST FORWARD COMMAND J308
REMOTE AUDIO MUTE J308
PRIMARY CUE PRESENT
PRIMARY CUE SENSOR
NORMAL
DEFEAT
SECONDARY (150Hz) CUE TONE PRESENT
EOM SELECT JUMPER
TERTIARY (8kHz) CUE TONE PRESENT
TIMER FREEZE JUMPER
BEG OF EOM
END OF EOM
TIMER FREEZE LATCH
FAST FLASH LATCH
SLOW FLASH LATCH
FAST FORWARD AT MUTE JUMPER
FAST FORWARD LATCH
MUTE LATCH
2 Hz CLOCK
TO CUE DISABLE (D3)
TO CLOCK DIVIDER RESET
TO CUE DISABLE (D2)
FLASH SYNCRO JUMPER
JUMPER IF MASTER OR INDIVIDUAL
OPEN IF SLAVE OR NO FLASH
J308 LAMP SYNCHRO I/O
J308 REMOTE FAST FORWARD INDICATOR
P301 FAST FORWARD LIGHT
P301 FAST FORWARD
P301 AUDIO ENABLE/MUTE
P301 AUDIO LIGHT
P301 TIMER FREEZE/COUNT
P301 RECORD LIGHT
+12V DIG
U12A LM339A
U14A U14B U14C U14D ULN2004
U15A U15B U15C ULN2004
U14E U14F ULN2004
U16A U16B U16C U16D U16E U16F 4584
U17A U17B U17C U17D 4071
U18A U18B 4011
U19A U19B 4001
U20A U20B U20C U20D 4081
U21A U21B U21C U21D 4071
U22A U22B U22C 4071
U26A U26B U26C 4073
U27A U27B 4538
U23A U23B U24A U24B U25A U25B U25C U25D 4013
U13A U13B U13C U13E U13F 4584
U18C U18D 4011
U19C U19D 4001
U22D 4071
D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D32 D33 D35 D36 D37 D38 D39 D42 D43 D44 D45 1N4148
D35 1N35
P302 J303 P303
P314 J314
P304 J304
P305 J305
P306 J306
P307 J307
P309 J309
DS2 DS3
R84 R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R122 R123 R124 R125 R126 R127 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142
C49 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C80 C81 C82 C83
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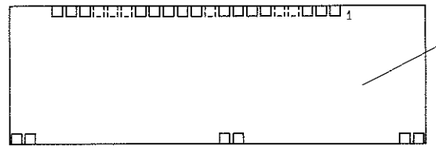
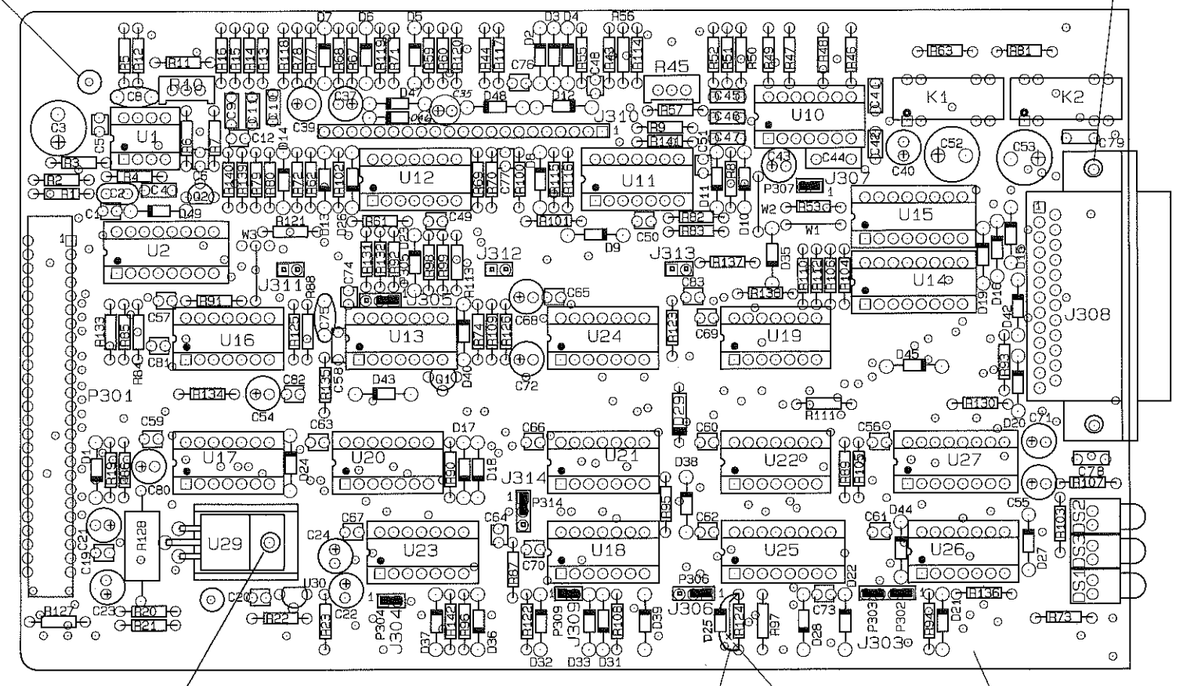
DWN. BY JAH 5-12-87
CHKD
ENG
PROJ. ENGR.
MFG.
TOLERANCE (DECIMAL) U.O.S. .x ± .030 .xx ± .015 .xxx ± .005 ANGLES ± 1°
MATERIAL SEE B/M 950-0035
FINISH
SEE DWG RA502-0000
NEXT ASSY. 900-9000-000
BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST
TITLE LOGIC MODULE
TYPE S SIZE D DWG. NO. 950-0035 REV M
MODEL PT-90 SCALE — SHEET 2 OF 2



220-0001, TO BE MOUNTED
IN J310, J311, J312 AND J313

MOUNT WITH:
420-6104
423-6002
423-6011
TYP. 2 PLCS.

MOUNT WITH:
420-4105
423-4002
423-4001
TYP. 2 PLCS.



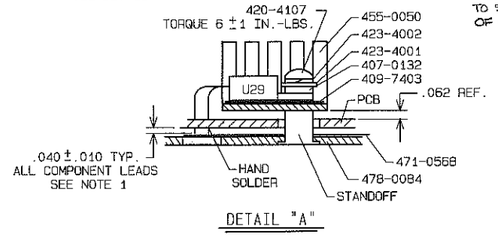
SEE DETAIL "A"

SOLDER JUMPER TO SOLDER SIDE OF BOARD

CUT TRACE GOING FROM TOP OF R124 TO FEED THRU

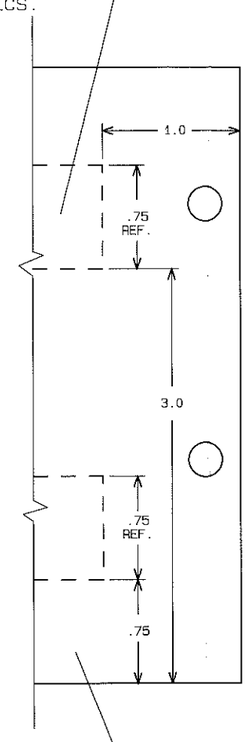
510-9004

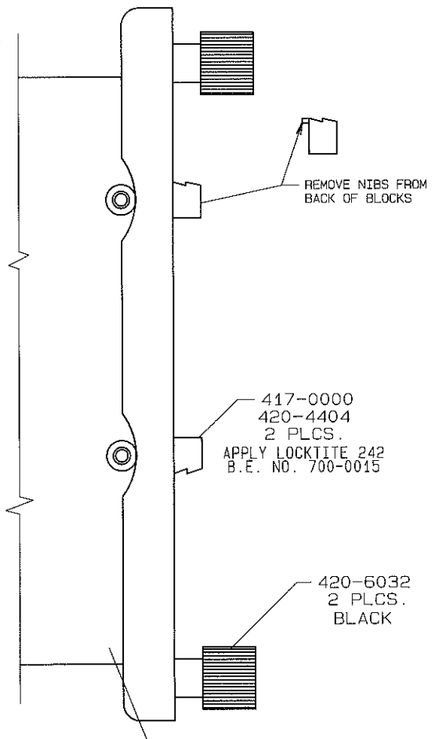
NOTE: CHG R124 TO BE # 100-1051
10K 1/4W 1%,
D25 IS BE# 202-0034 1N34



DETAIL "A"

INSTALL 5" ± .2 LG. TAPE 700-0148
BETWEEN PHENOLIC 471-0569 AND MODULE 478-0084.
PLACEMENT TOL. ± .2





471-0568
TO BE INSTALLED BETWEEN
PCB AND 478-0084

478-0084

NOTES:
1. TRIM ALL COMPONENT LEADS TO .040 ± .010
2. TEST PCB BEFORE SHEET METAL IS ADDED
3. SEE SCHEMATIC SD950-0035
4. *U29 TO BE INSTALLED AFTER ASSEMBLY OF 478-0084 BRACKET TO 510-9004 PCB.*

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN BY	MERK 1-19-87	MATERIAL: SEE B/M 950-0035
CHKD		
ME	5-15-87 J.H. STEINKAMP	FINISH
PROJ. ENGR.	JAC 5-15-87	
MFG.	R. BROSE 5-15-87	NEXT ASSY 900-9000-000

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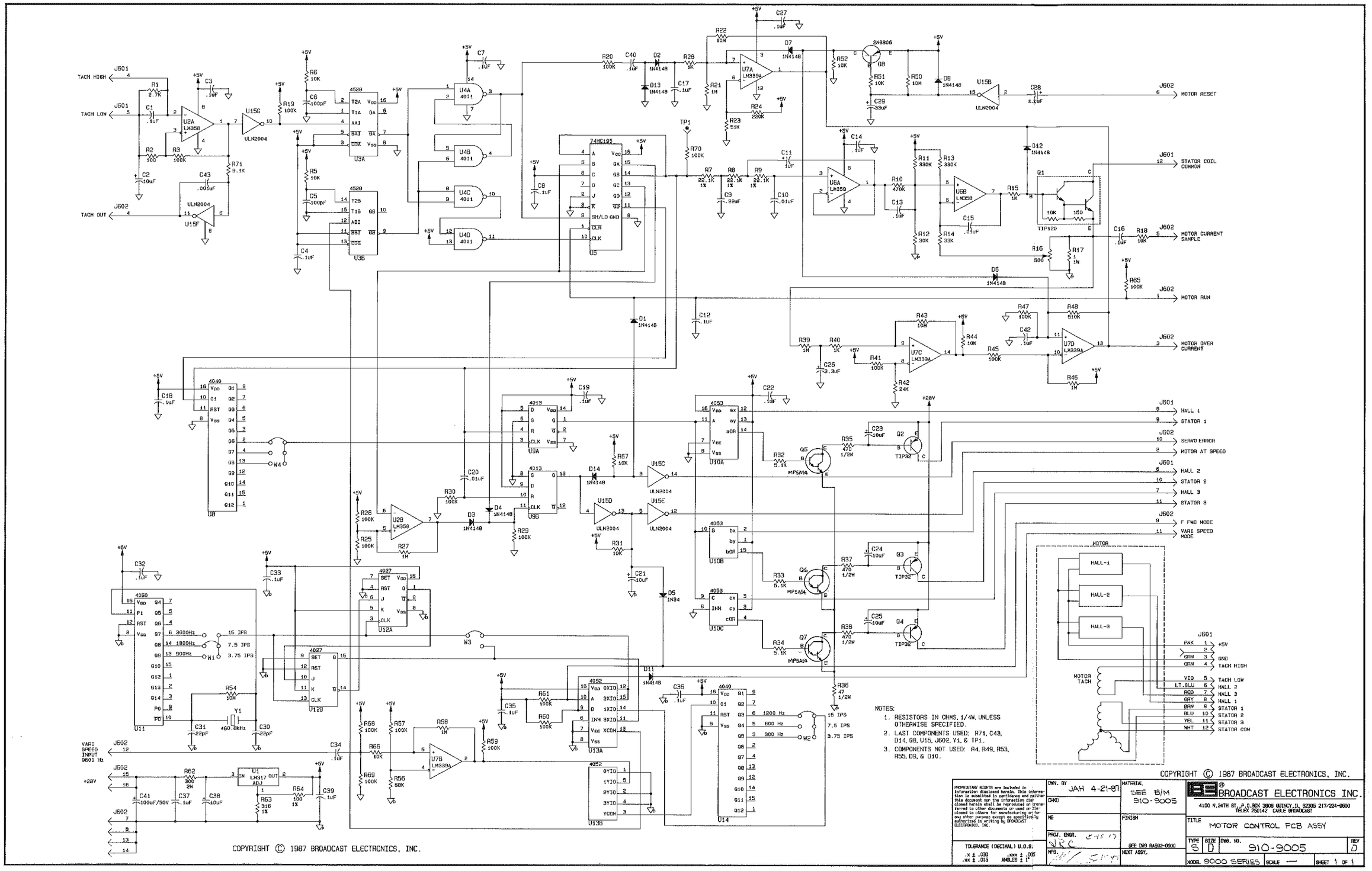
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE: LOGIC MODULE ASSEMBLY

TYPE	SIZE	DWG. NO.	REV
A	D	950-0035	N

MODEL PT90PS SCALE 2/1 SHEET 1 OF 1


TACH HIGH
TACH LOW
TACH OUT
MOTOR RESET
STATOR COIL COMMON
MOTOR CURRENT SAMPLE
MOTOR RUN
MOTOR OVER CURRENT
HALL 1
STATOR 1
SERVO ERROR
MOTOR AT SPEED
HALL 2
STATOR 2
HALL 3
STATOR 3
F FWD MODE
VARI SPEED MODE
VARI SPEED INPUT 9600 Hz
+28V
15 IPS
7.5 IPS
3.75 IPS
MOTOR
HALL-1
HALL-2
HALL-3
MOTOR TACH
+5V
GND
TACH HIGH
TACH LOW
HALL 2
HALL 3
HALL 1
STATOR 1
STATOR 2
STATOR 3
STATOR COM
NOTES:
1. RESISTORS IN OHMS, 1/4W, UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: R71, C43, D14, Q8, U15, J602, Y1, & TP1.
3. COMPONENTS NOT USED: R4, R49, R53, R55, D9, & D10.
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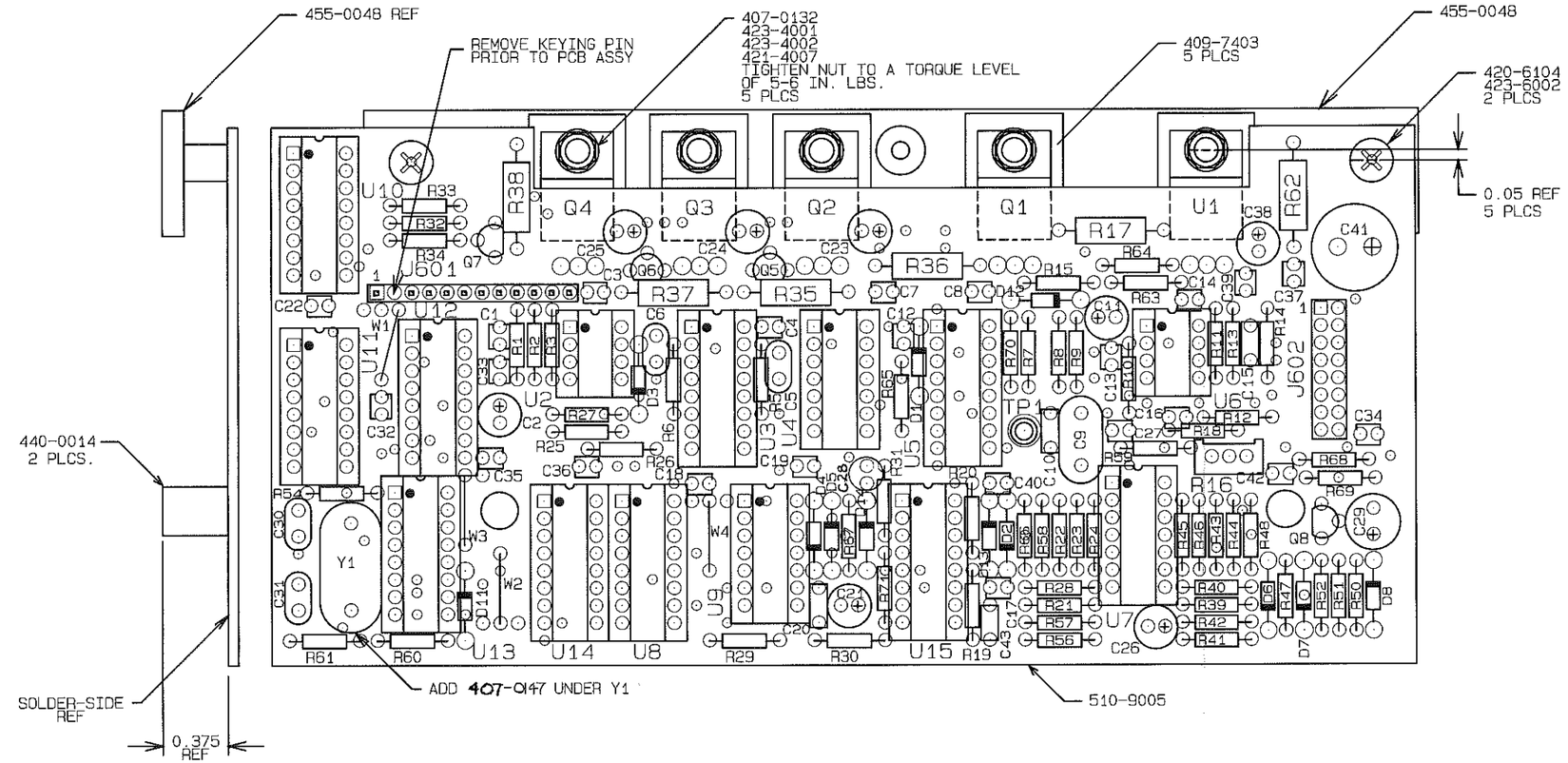
BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST
MOTOR CONTROL PCB ASSY
910-9005
MODEL 9000 SERIES
SHEET 1 OF 1



NOTES:

1. SEE SCHEMATIC NO. SD910-9005.

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN BY M. HAYDEN	DATE 11-19-86	MATERIAL SEE B/M 910-9005
CHKD		
ME	12-4-87	FINISH —
PROJ ENGR		
MFG		NEXT ASSY

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST. QUINCY, IL. 62305 217/224-9600
TELEX 250142 CABLE "BROADCAST"

TITLE PCB ASSEMBLY
MOTOR CONTROL BOARD

TYPE	SIZE	DWG. NO.	REV
A	C	910-9005	D

MODEL PT90 | SCALE 2/1 | SHEET 1 OF 1

NOT PART OF PCB

117 SHOWN WHT
F1 117, .5A
230, .25A
S201
S202
IEC CONNECTOR
TO AC
T1
YEL
ORN
BRN
BLK
BLU

P202
1 +20Vac
2 CT
3 -20Vac
4 +25.6Vac
5 +25.6Vac RETURN
7 +9Vac
8 +9Vac RETURN

J202
TP1
TP2
TP3
TP4
TP5
TP6
R11 10K
R12 10K
R13 10K
R14 10K
R16 10K
D1 1N4005
D2 1N4005
D3 1N4005
D4 1N4005
C1 2200/35V
C2 2200/35V
+22.5V
Q5 TIP31
R1 470
D15 1N4750
C3 10/50V
D5 MR502
D6 MR502
D7 MR502
D8 MR502
C4 4700/50V
+28V
D9 MR502
D10 MR502
D11 MR502
D12 MR502
C5 10,000/16V

P201
36
35
16
15
19
20
39
40
27
28
8
21
22
23
24
9
29
30
10
31
32

+10V
10V RETURN
RECORD PLAY ONLY

LAMP SUPPLY +28V
+28V
PART OF BACK PANEL
IC-1 LM317 TO-3
IN
OUT
ADJ
R8 15
R9 50
R7 5.0 1% 1W
P201 SOLENOID
P201 DRIVE (+)
28V RETURN
SPLICE P201 12
D16 1N4148
Q4 TIP125
C8 1/50V
R6 10K
Q3 2N3904
D13 1N4148
D14 1N4148
R4 100K
R5 10K
C7 1/50V

SOLENOID ENERGIZE P201 34 14
Q1 2N3904
R2 68K
R3 10K
C6 100PF
Q2 TIP120
P201 SOLENOID
P201 RETURN (-)

TO REAR PANEL FEED THROUGH
E1 CIRCUIT GND
AC GROUND
E4
E3 TO REAR PANEL CHASSIS STUD
E2
SHIELDS
5 P201
6 P201
7 P201
25 P201
26 P201

P201 11
P201 13
P201 33
P201 37
P201 38
P201 17
P201 18

FOR UNITED KINGDOM
E1
E3
E4
E2

NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5%: ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED:
   C8, D16, E4, F1, J203, Q5, R16, S202, T1, TP5.
   COMPONENTS NOT USED: R10, R15.
3. SEE PCB ASSEMBLY
   AC950-0032-001 SHEET 1.
   AD950-0032-001 SHEET 2.

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

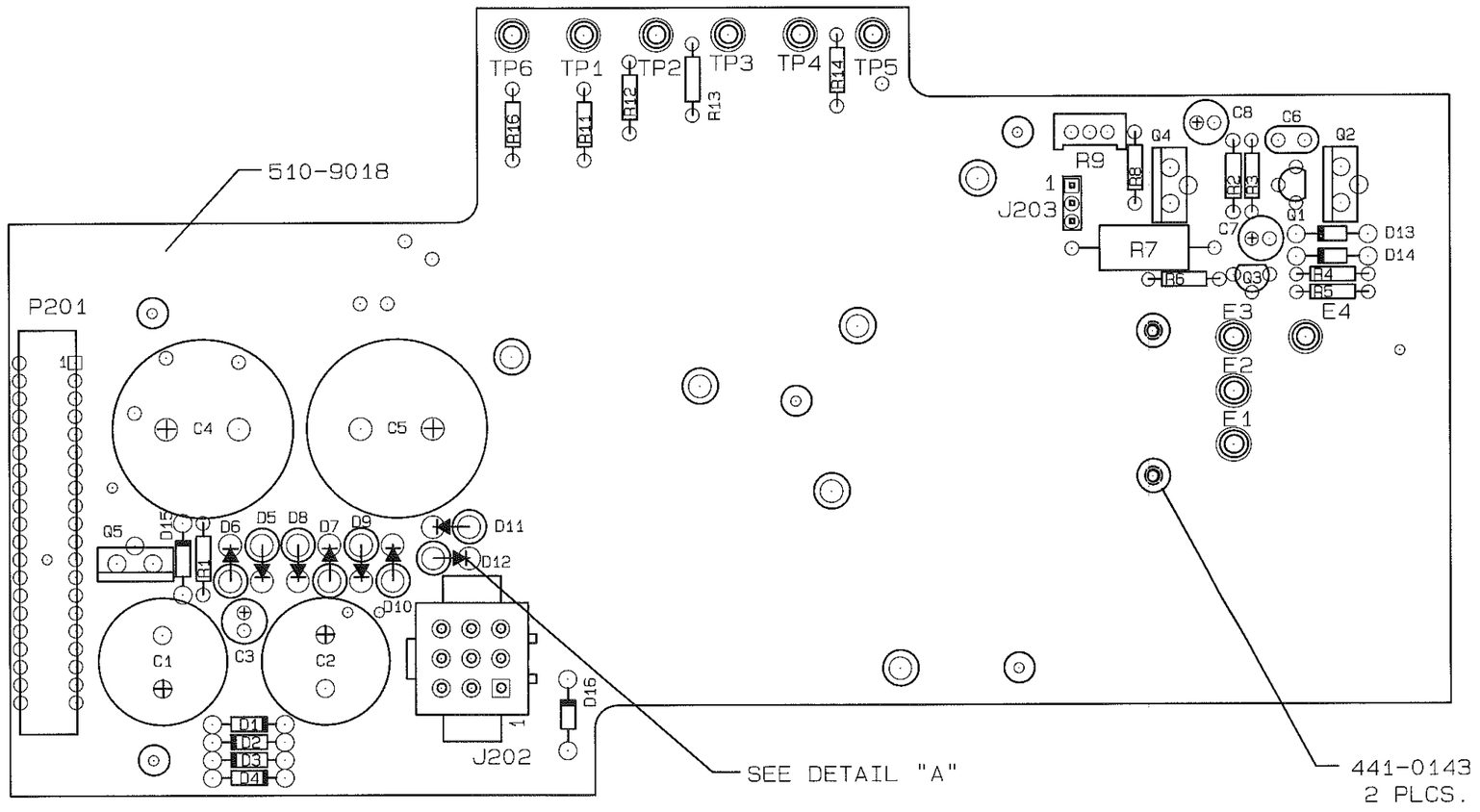
DWN BY	MERK 11-12-87
CHKD	
ME	
PROJ. ENGR.	
MFG	
MATERIAL	SEE B/M 950-0032-001
FINISH	
NEXT ASSY	

BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9500
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

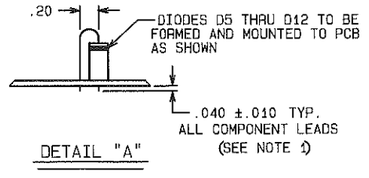
TITLE: SCHEMATIC POWER SUPPLY MODULE

TYPE	SIZE	DWG.NO.	REV
S	C	950-0032-001	A

MODEL PT90RP SCALE NONE SHEET 1 OF 1



NOTE:
1. TRIM ALL COMPONENT LEADS TO .040 ±.010
2. SEE SCHEMATIC SC950-0032-001.
3. SEE AD950-0032-001 FOR SHEET 2.



DETAIL "A"

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN BY MERK 11-12-87
CHKD
ME 6-27-88
PROJ. ENGR. 4-21-88
MFG 4-27-88

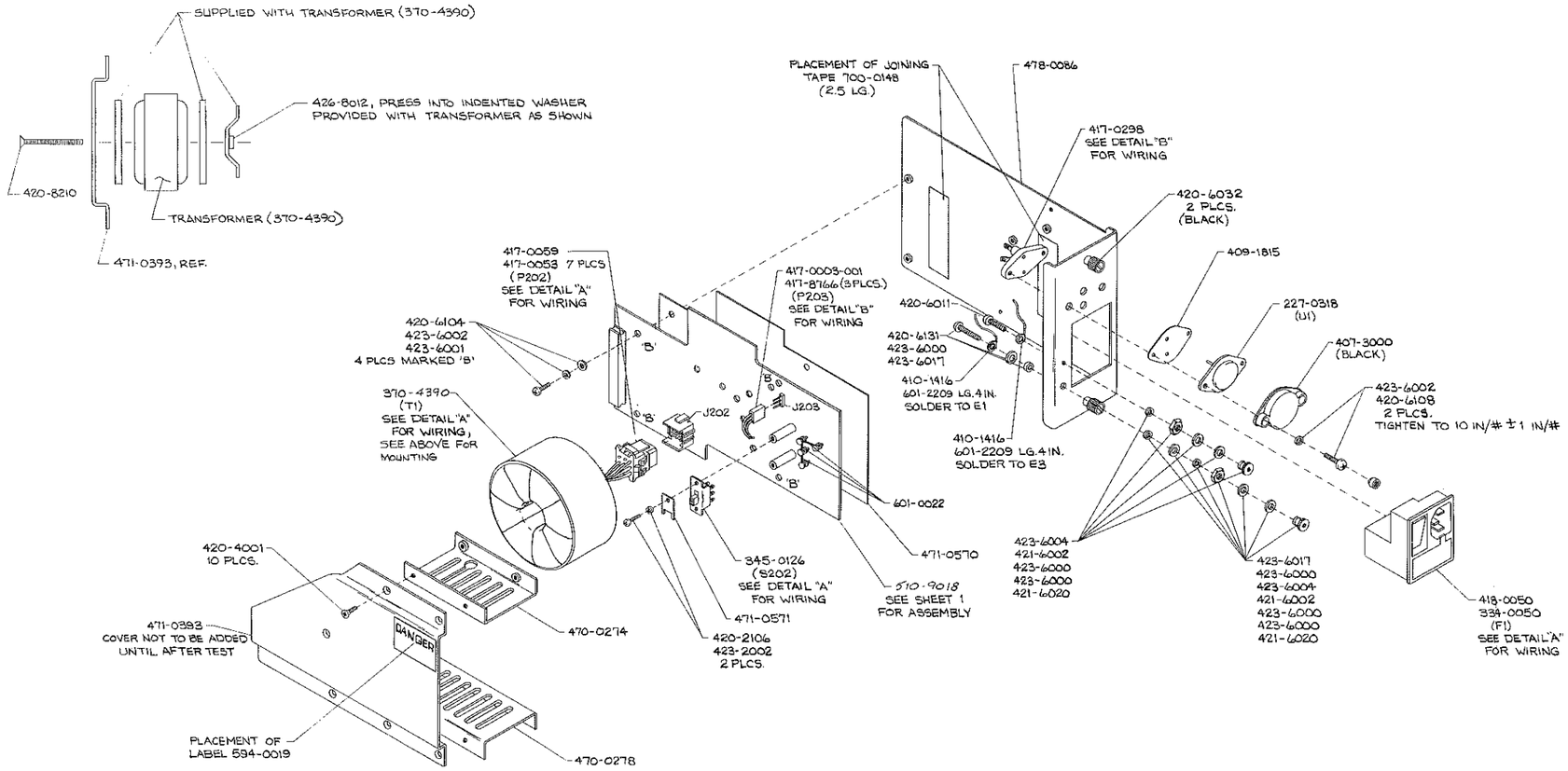
MATERIAL SEE B/M 950-0032-001
FINISH
NEXT ASSY

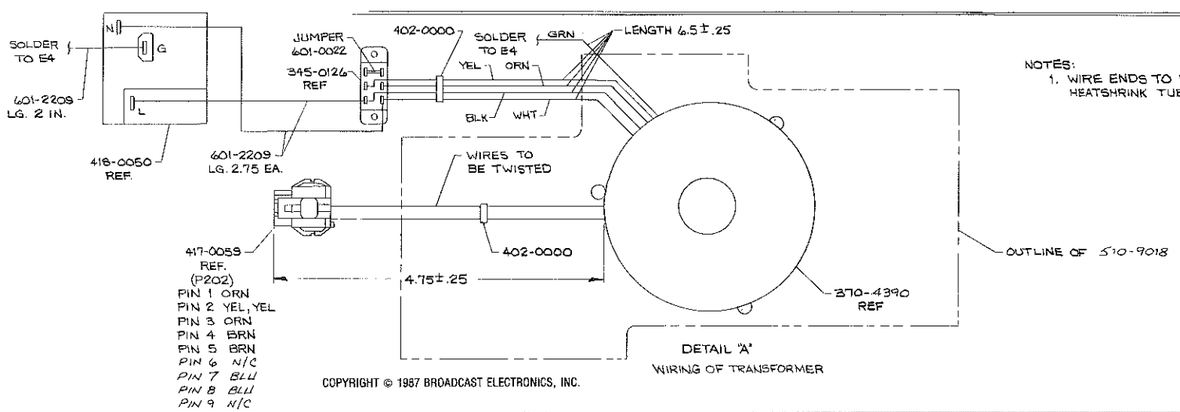
BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY POWER SUPPLY MODULE

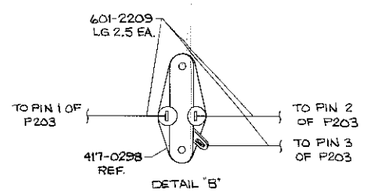
TYPE	SIZE	DWG.NO.	REV
A	C	950-0032-001	B

MODEL PT90RP SCALE 2/1 SHEET 1 OF 2





NOTES:
1. WIRE ENDS TO BE INSULATED USING HEATSHRINK TUBING 611-1250



NOTE
WIRES TO BE INSULATED USING HEATSHRINK TUBING 611-1250

SHEET 1 OF DRAWING IS "C" SIZE

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 11-16-87
CHKD
ME
PROJ. ENGR. DRC 4-27-88
MFG.
MATERIAL SEE B/M 950-0032-001
FINISH
SEE DWG RA592-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
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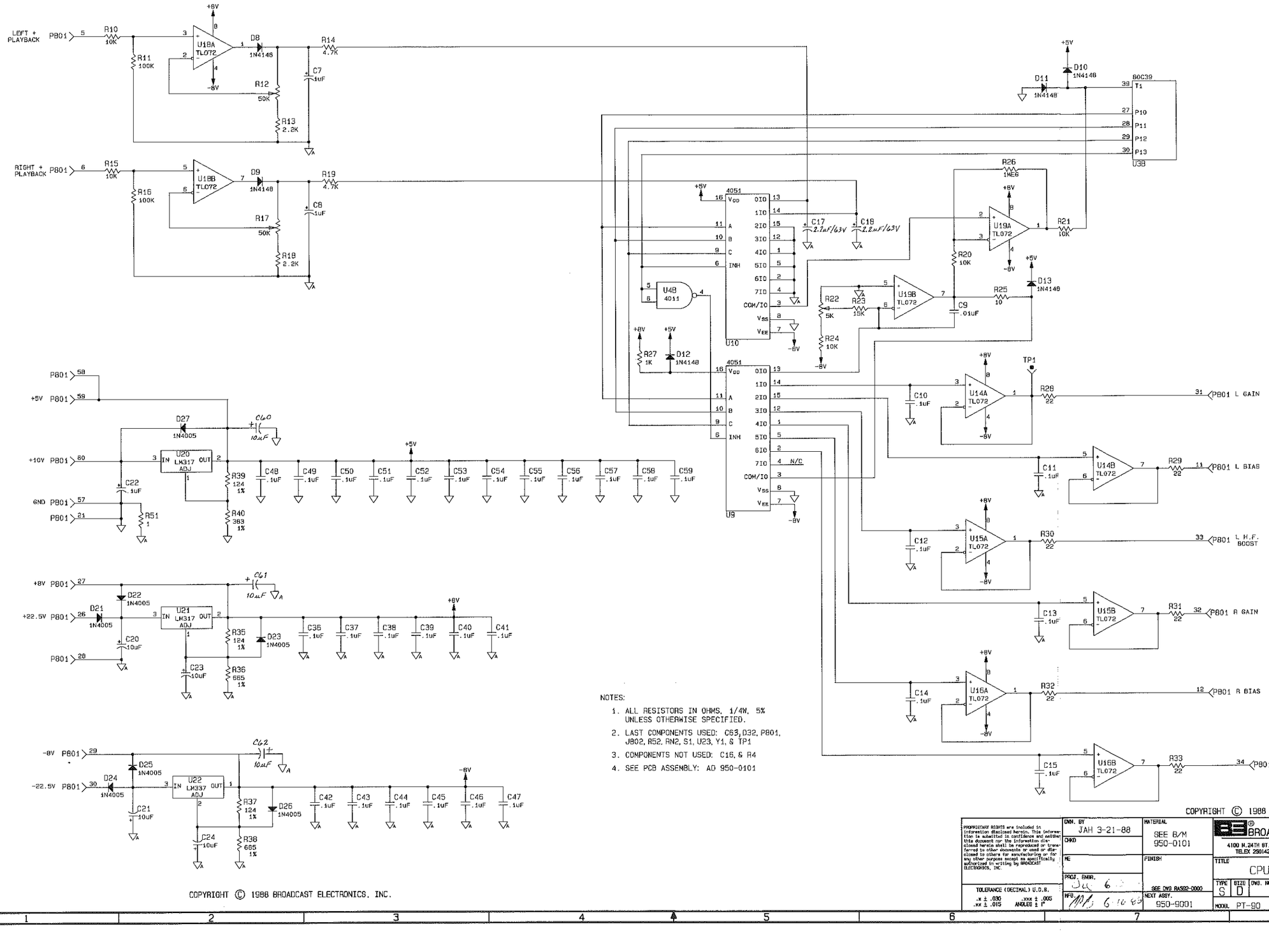
TELEX 250142 CABLE BROADCAST

TITLE ASSEMBLY POWER SUPPLY MODULE

TYPE	SIZE	DWG. NO.	REV
A	D	950-0032-001	B

MODEL FT90RP SCALE 1/2 SHEET 2 OF 2



NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: C63, D32, P801, J802, R52, RN2, S1, U23, Y1, & TP1
3. COMPONENTS NOT USED: C16, & R4
4. SEE PCB ASSEMBLY: AD 950-0101

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 3-21-88
CHKD
ME
PROJ. ENGR. JAH 6
MFG. MP 6 10 88

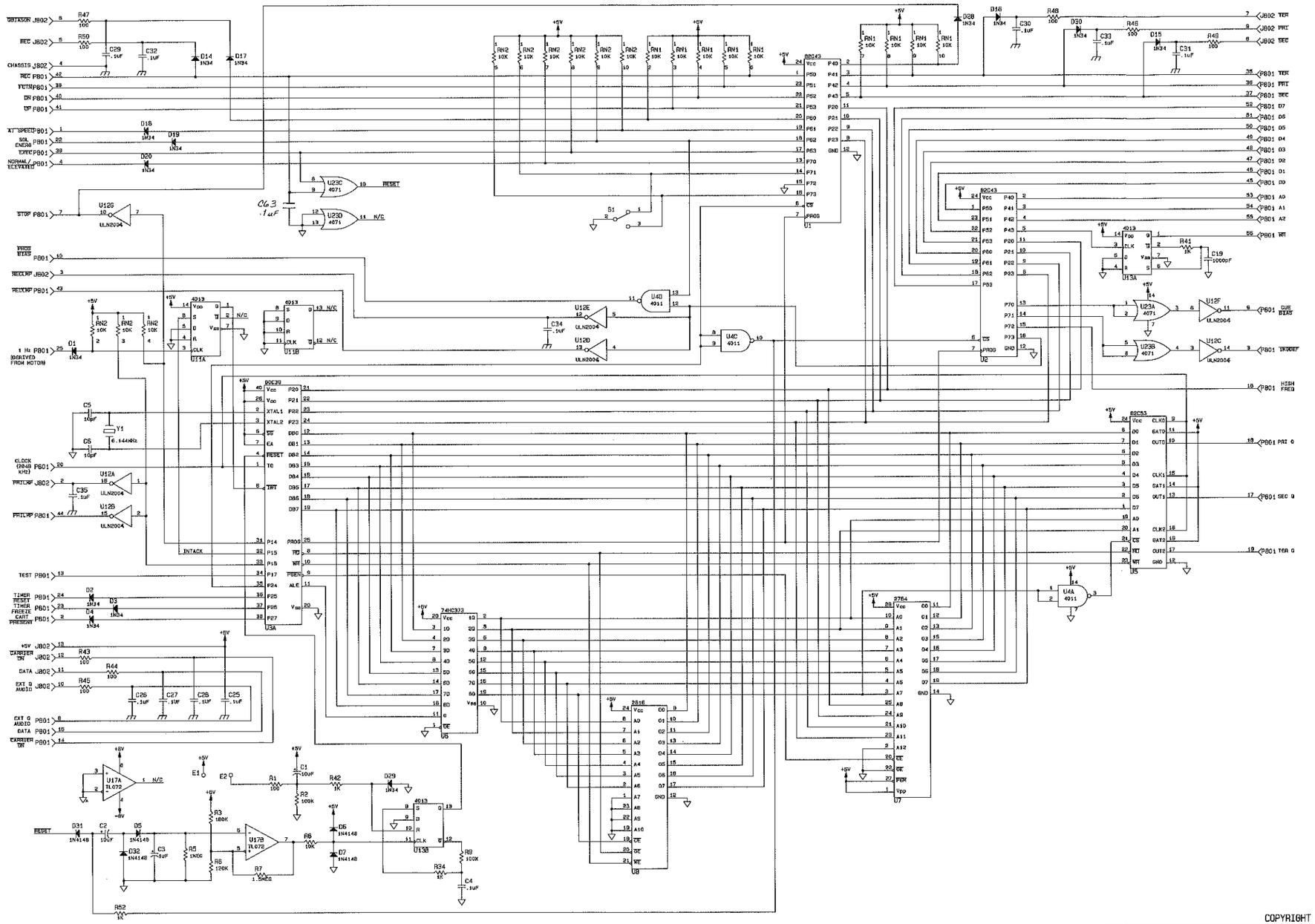
MATERIAL SEE B/M 950-0101
FINISH
SEE DWG RA552-0000
NEXT ASSY. 950-9001

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3506 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE CPU MODULE

TYPE S | SIZE D | DWG. NO. 950-0101 | REV C

MODEL PT-90 | SCALE NONE | SHEET 1 OF 2


OBTASOR J802
REC J802
CHASSIS J802
REC P801
VOUTP801
DN P801
UP P801
AT SPEED P801
SBL ENBSB P801
EXEC P801
NORMAL / ELEVATED P801
STOP P801
PROG BIAS P801
RECCMP J802
REXCMP P801
1 Hz P801 (DERIVED FROM MOTOR)
CLOCK (2048 KHz) P801
PRICMP J802
PRILMP P801
TEST P801
TIMER RESET P801
TIMER FREEZE P801
CART PRESENT P801
+5V J802
CARRIER ON J802
DATA J802
EXT Q AUDIO J802
EXT Q AUDIO P801
DATA P801
CARRIER ON P801
INTACK
RESET
C63 .1uF
RESET
HIGH FREQ
TER
PRI
SEC
D7
D6
D5
D4
D3
D2
D1
D0
A0
A1
A2
WR
GUE BIAS
TKODEF
PRI Q
SEC Q
TER Q
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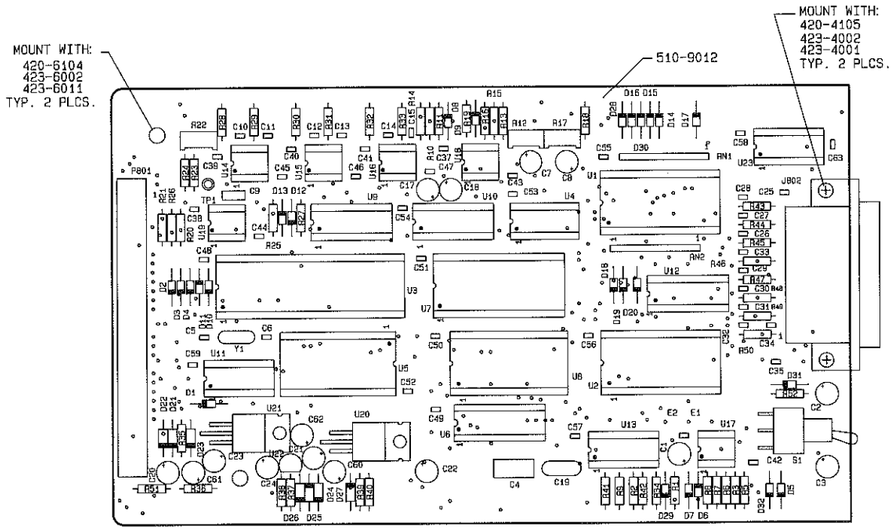
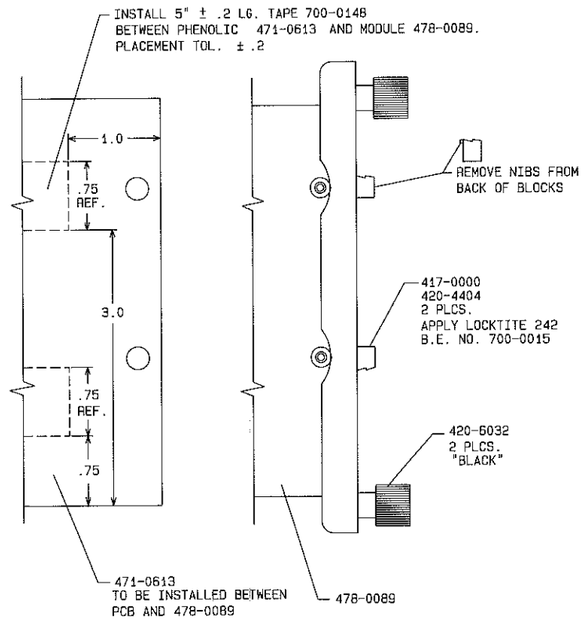
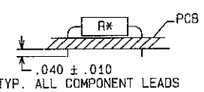
TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°
DWN. BY JAH 3-21-88
CHKD
ENG
PROJ. ENGR.
MFG
MATERIAL SEE B/M 950-0101
FINISH
SEE DWG RA592-0000
NEXT ASSY. 950-9001
BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607
TITLE CPU MODULE
TYPE S SIZE D DWG. NO. 950-0101 REV C
MODEL PT-90 SCALE NONE SHEET 2 OF 2







DETAIL "A"

NOTES:
1. TRIM ALL COMPONENTS LEADS TO .040 ± .010, SEE DETAIL "A"
2. TEST PCB BEFORE SHEET METAL IS ADDED.
3. SEE SCHEMATIC SD950-0101

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN. BY JAH 9-9-91
CHKD 9-9-91
M. HAYDEN
ME
PROJ. ENGR. 9-9-91
J. TUCKER
MFG.

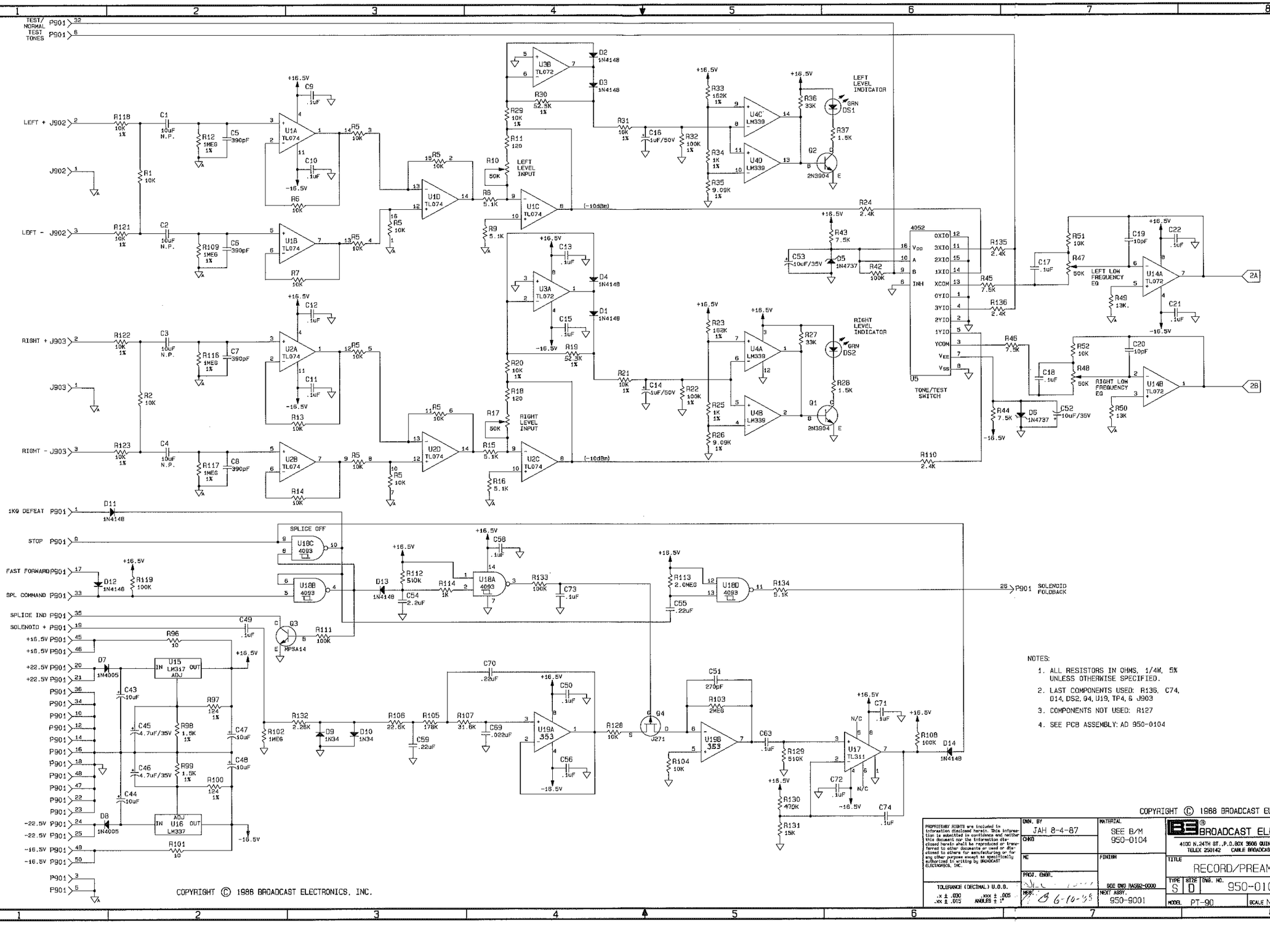
MATERIAL SEE B/M 950-0101
FINISH
SEE DWG RA592-0000
NEXT ASSY. 950-9001

BROADCAST ELECTRONICS INC.
4100 N.24TH ST. P.O.BOX 3606 QUINCY, IL. 62305 PH. 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE PCB ASSEMBLY
CPU BD

TYPE A | SIZE C | DWG No. 950-0101 | REV E

MODEL PT90RP | SCALE 1=1 | SHEET 1 OF 1


TEST/NORMAL TEST TONES P901
LEFT + J902
LEFT - J902
RIGHT + J903
RIGHT - J903
1KΩ DEFEAT P901
STOP P901
FAST FORWARD P901
SPL COMMAND P901
SPLICE IND P901
SOLENOID + P901
+16.5V P901
+22.5V P901
-22.5V P901
-16.5V P901
LEFT LEVEL INPUT
RIGHT LEVEL INPUT
LEFT LEVEL INDICATOR
RIGHT LEVEL INDICATOR
TONE/TEST SWITCH
LEFT LOW FREQUENCY EQ
RIGHT LOW FREQUENCY EQ
SPLICE OFF
P901 SOLENOID FOLDBACK
2A
2B
NOTES:
1. ALL RESISTORS IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: R135, C74, D14, DS2, Q4, U19, TP4, & J903
3. COMPONENTS NOT USED: R127
4. SEE PCB ASSEMBLY: AD 950-0104
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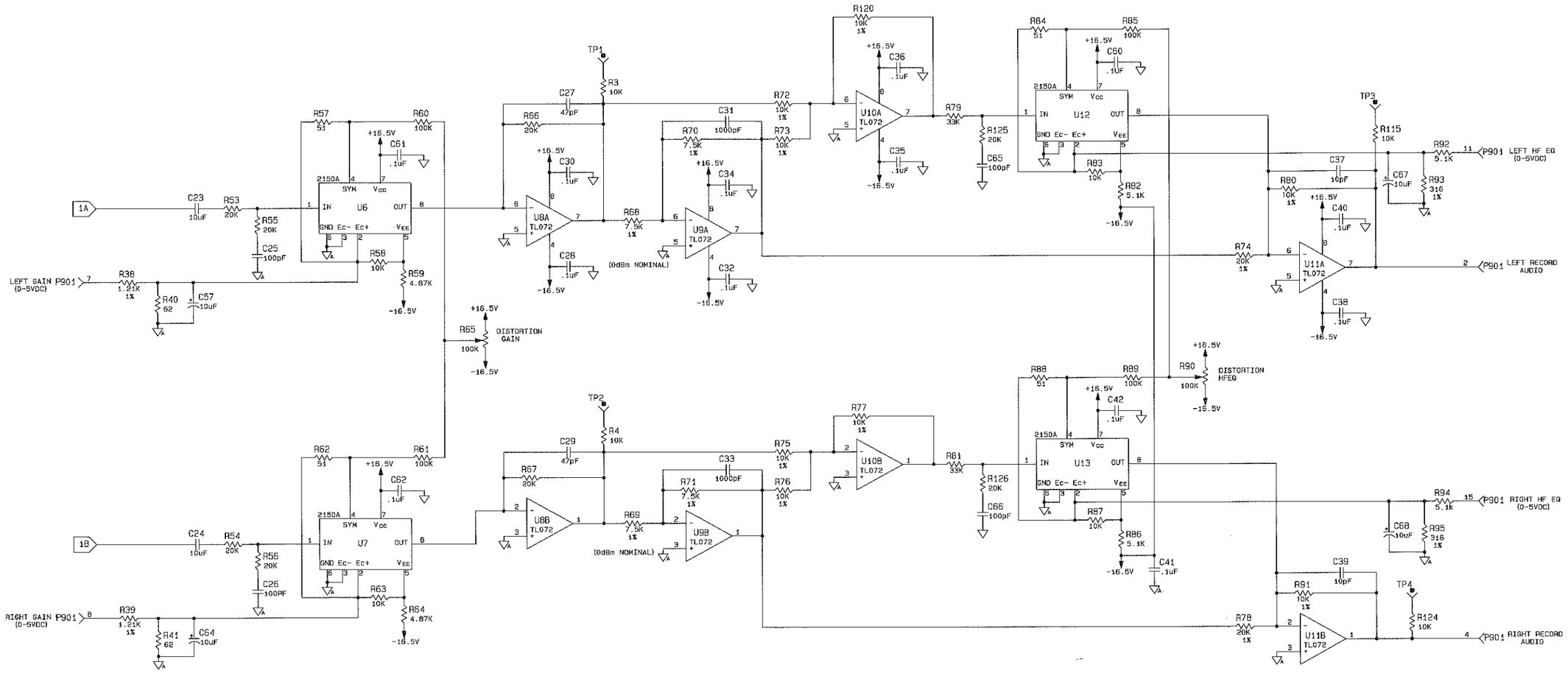
4100 N.24TH ST.,P.O.BOX 3506 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607
TITLE RECORD/PREAMP MODULE
DWG. NO. 950-0104
REV C
MODEL PT-90
SCALE NONE
SHEET 1 OF 2



TOLERANCE (DECIMAL) U.O.S.
.xx ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

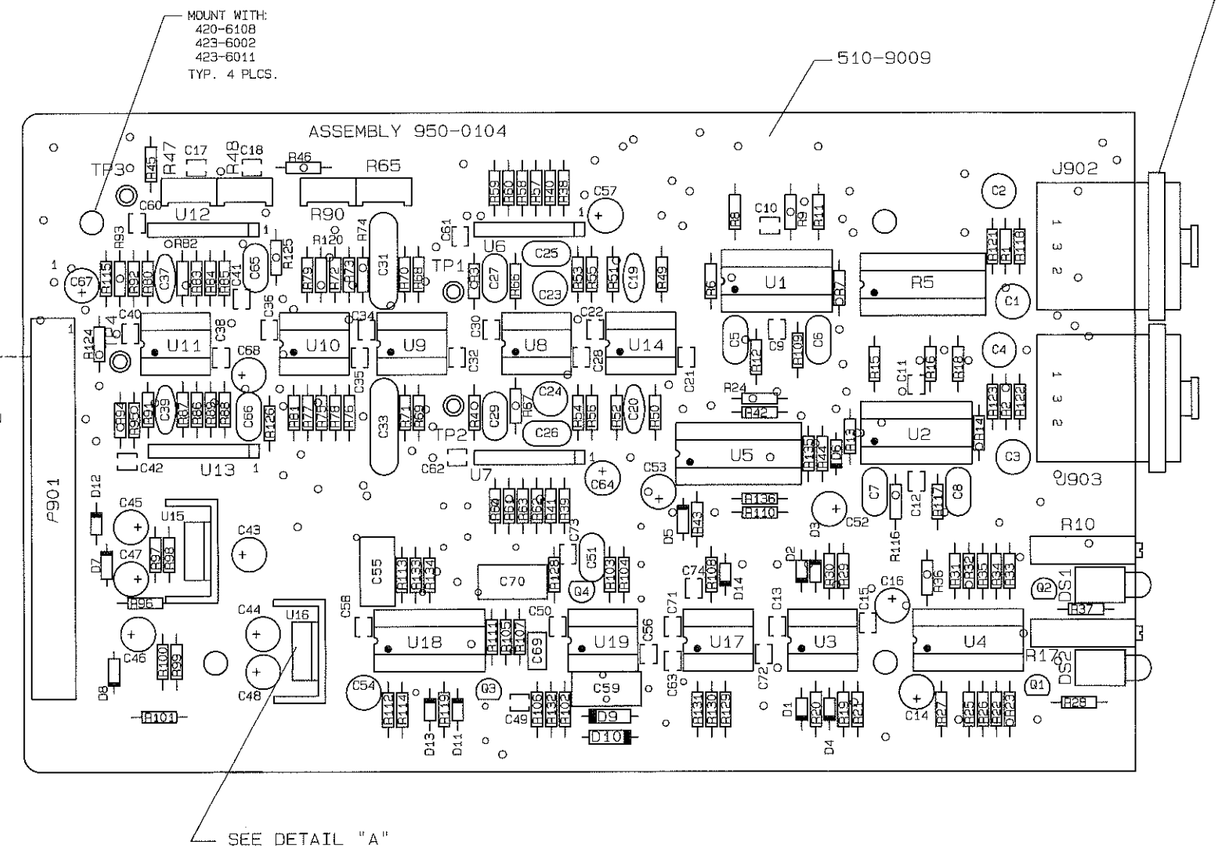
DWN. BY	JAH 8-4-87
CHKD	
ME	
PROJ. ENGR.	
MFG.	6-16-87
MATERIAL	SEE B/M 950-0104
FINISH	SEE DWG RA5R2-0000
NEXT ASSY.	950-9001

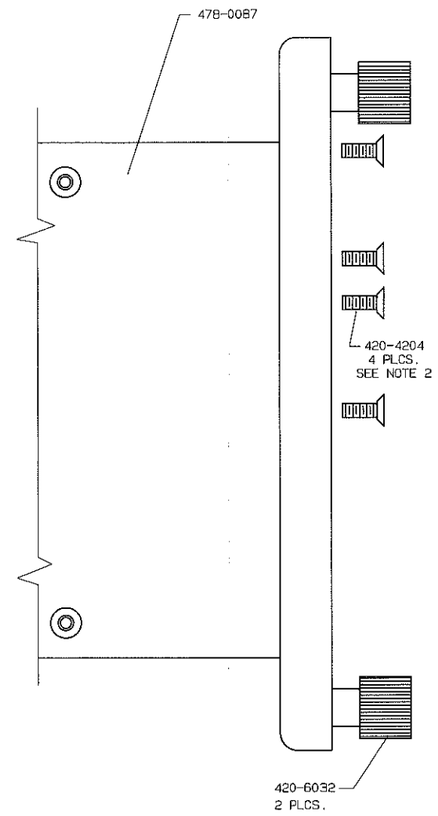
BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

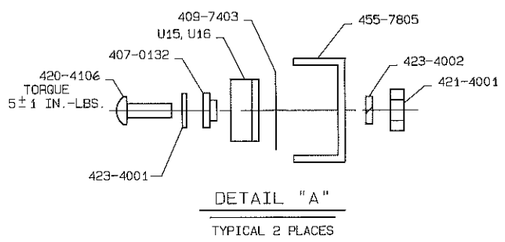
TITLE: RECORD/PREAMP MODULE

TYPE	SIZE	DWG. NO.	REV
S	D	950-0104	C

MODEL PT-90 | SCALE NONE | SHEET 2 OF 2







NOTES:

1. MOUNT J902 AND J903 HOUSINGS TO 478-0087 BEFORE SOLDERING TO PCB.
2. APPLY LOCKTITE 242 700-0015 TO 420-4204, 4 PLCS.
3. TEST PCB BEFORE ADDING SHEETMETAL 478-0087.

TOLERANCE DECIMAL U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN BY	MERK 12-3-87
CHKD	
ME PROJ. ENGR.	6-10-88
MFG	6-16-88
MATERIAL	SEE B/M 950-0104
FINISH	
NEXT ASSY	950-9001

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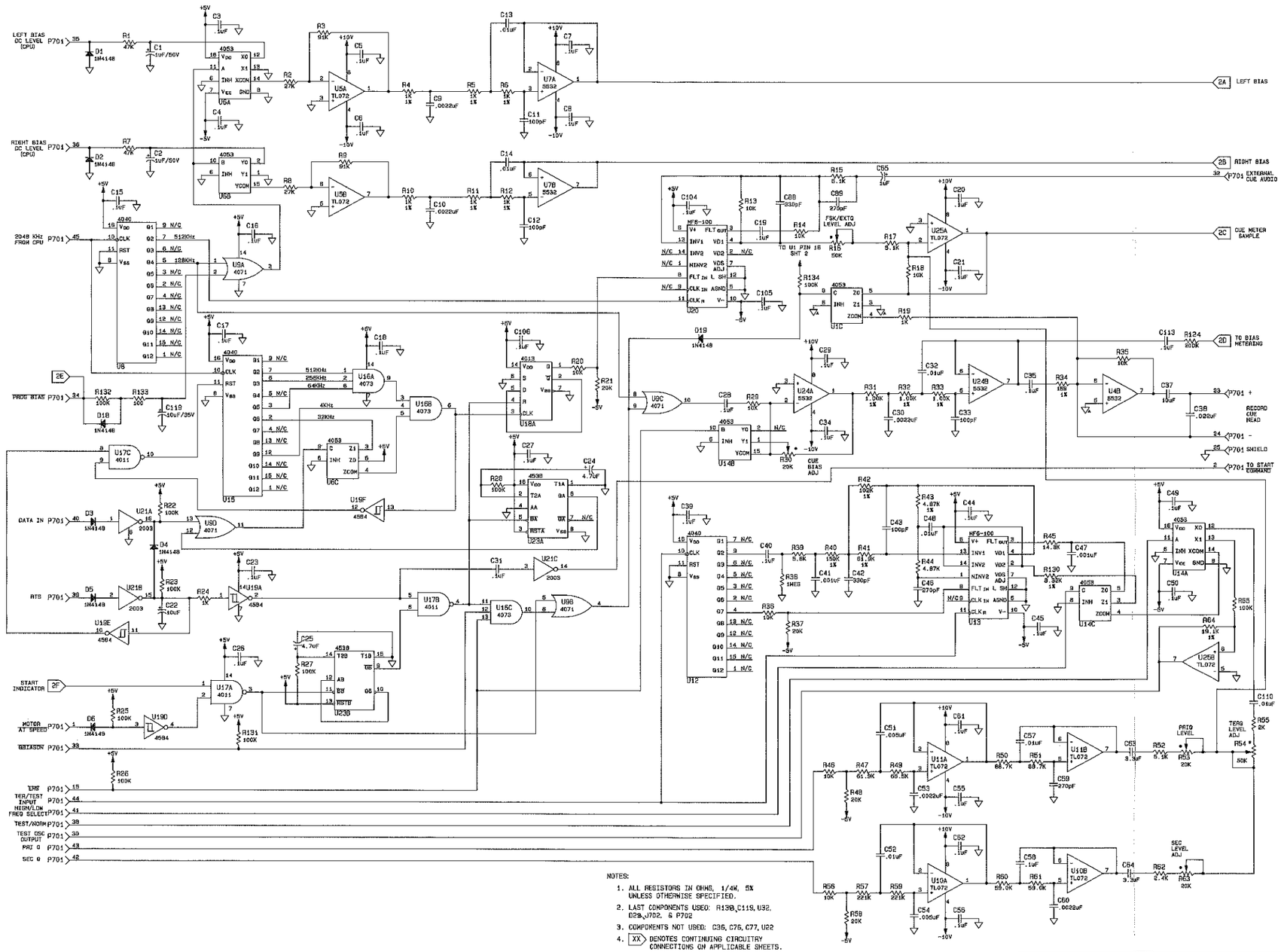
TELEX 250142 CABLE BRDCAST FAX 217/224-9607

TITLE: PCB ASSEMBLY- RECORD PREAMP

TYPE	SIZE	DWG.NO.	REV
A	D	950-0104	F

MODEL PTS9RP/RPS SCALE 2/1 SHEET 1 OF 1



NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: R139,C119, U32, D28,J702, & P702
3. COMPONENTS NOT USED: C35, C75, C77, U22
4. XX DENOTES CONTINUING CIRCUITRY CONNECTIONS ON APPLICABLE SHEETS.
5. SEE PCB ASSEMBLY: AD 950-0102

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY	JAH 10-27-87
CHKD	
MFG	
PROJ. ENGR.	
MATERIAL	SEE B/M 950-0102
FINISH	
NEXT ASSY.	950-9001

SEE DWG RA5B2-0000

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TITLE: RECORD/BIAS MODULE

TYPE	SIZE	DWG. NO.	REV
S	D	950-0102	E

MODEL PT-90 SCALE NONE SHEET 1 OF 2

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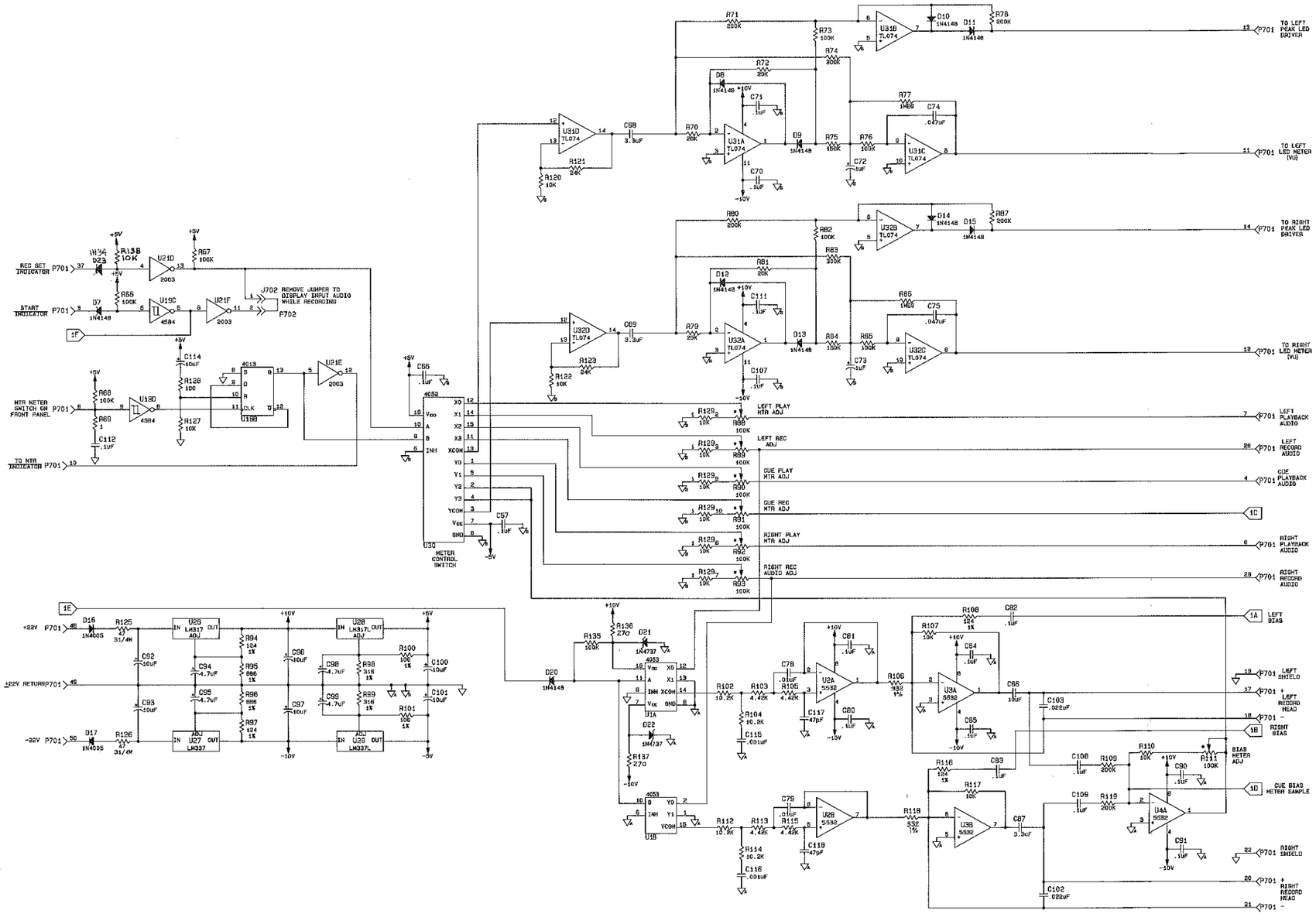

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN. BY JAH 10-27-87
CHKD MH 7-5-88
ME
PROJ. ENGR.
MFG
NEXT ASSY. 950-9001

MATERIAL SEE B/M 950-0102
FINISH
DO NOT SCALE DRAWING

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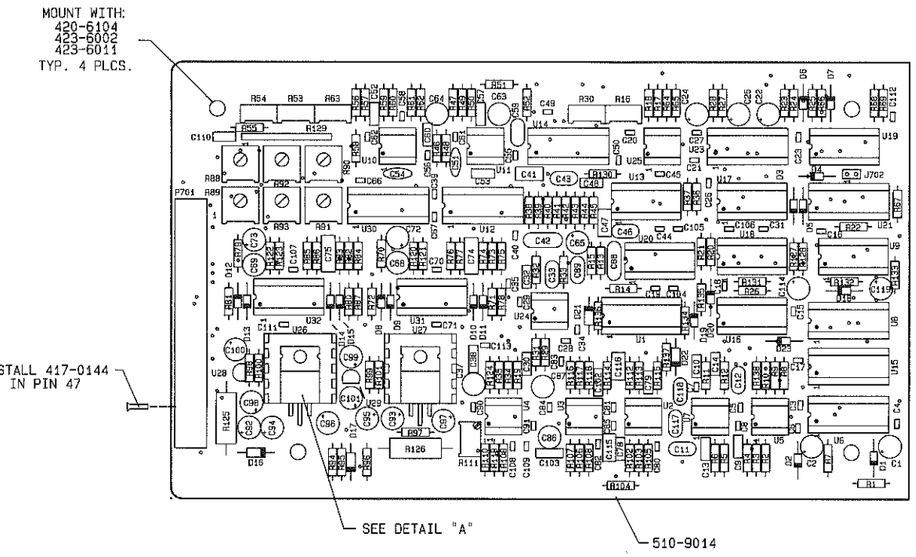
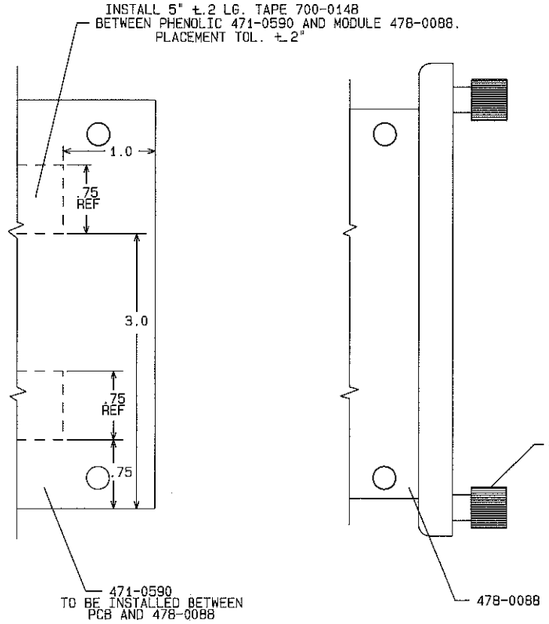
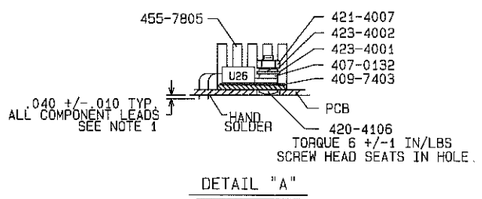
TITLE RECORD/BIAS MODULE

TYPE S SIZE D DWG. NO. 950-0102 REV E

MODEL PT-90 SCALE NONE SHEET 2 OF 2







DETAIL "A"

NOTES:

1. TRIM ALL COMPONENT LEADS TO .040 +/- .010 IN.
2. TEST PCB BEFORE SHEET METAL IS ADDED.
3. SEE SCHEMATIC SD950-0102.

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN. BY	MERK 12-7-87
CHKD	MH 7-5-88
ME	JHS 7-1-88
PROJ. ENGR.	JRC 6-29-88
MFG.	PRB 7-1-88

MATERIAL	SEE BOM 950-0102
FINISH	
	SEE DWG RA592-0000
NEXT ASSY.	950-9001

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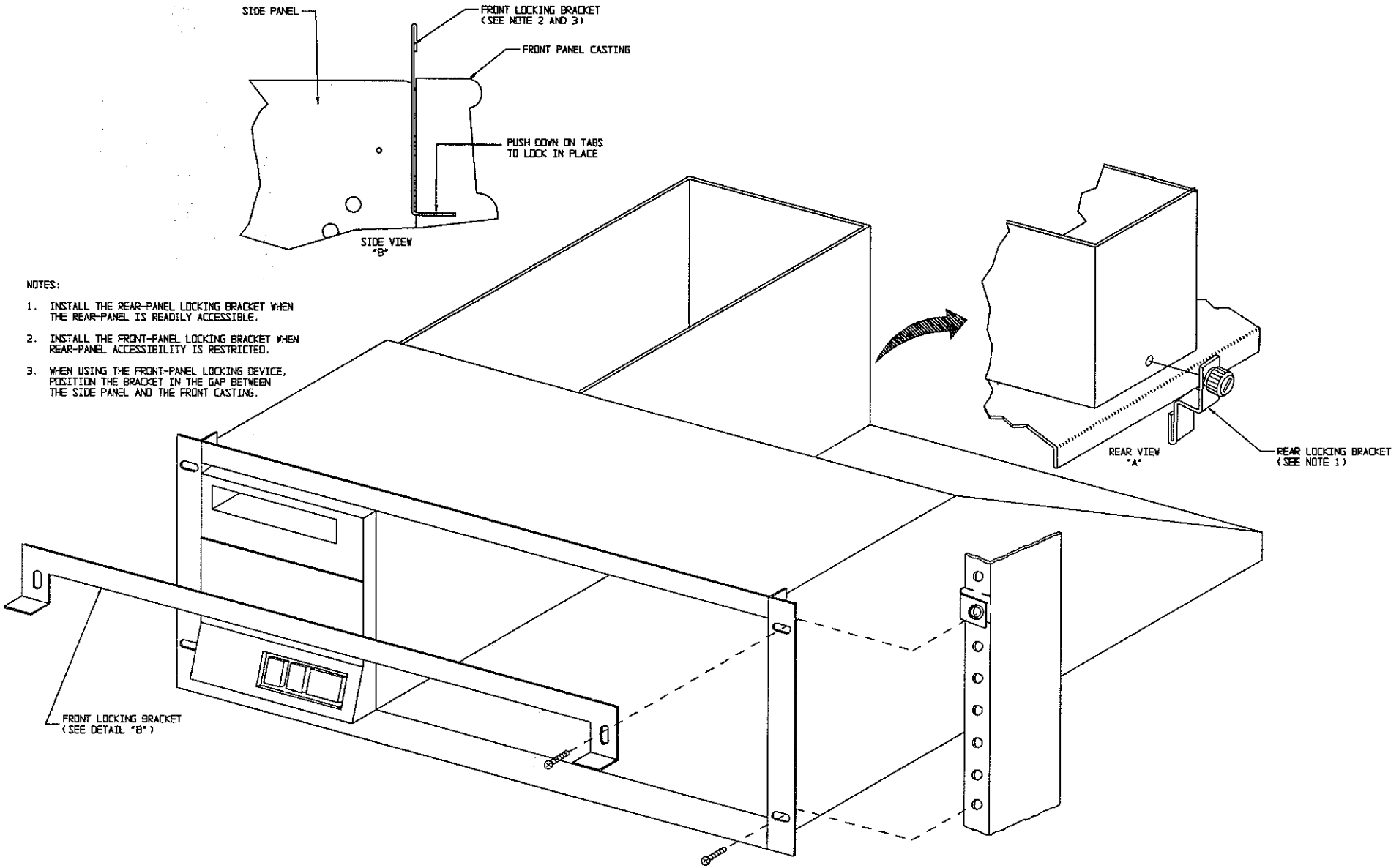
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE	PCB ASSEMBLY RECORD BIAS		
TYPE A	SIZE C	DWG No. 950-0102	REV I
MODEL PT90RPS		SCALE 1:1	SHEET 1 OF 1



597-9000-160

FIGURE 7–27. PT–90 RACK ASSEMBLY DIAGRAM

PRODUCT WARRANTY

LIMITED TWO YEAR

While this warranty gives Purchaser specific legal rights, which terminate two (2) years (one year on turntable, cartridge and blower motors) from the date of shipment, Purchaser may also have other rights which vary state to state.

Broadcast Electronics, Inc. ("Seller") hereby warrants cartridge machines, consoles, and other new Equipment manufactured by Seller against any defects in material or workmanship at the time of delivery thereof, that develop under normal use within a period of two (2) years (one year for turntable, cartridge and blower motors) from the date of shipment, as such term is defined herein. Other manufacturer's and suppliers' Equipment and services, if any, including electronic tubes, solid state devices, transmission line, antennas, towers, related equipment and installation and erection services, shall carry only such manufacturer's or suppliers' standard warranty. This warranty extends to the original user and any subsequent purchaser during the warranty period. Seller's sole responsibility with respect to any equipment or parts not conforming to this warranty is to replace such equipment or parts upon the return thereof F.O.B. Seller's factory or authorized repair depot within the period aforesaid.

In the event of replacement pursuant to the foregoing warranty, only the unexpired portion of the warranty from the time of the original purchase will remain in effect for any such replacement. However, the warranty period will be extended for the length of time that Purchaser is without the services of the Equipment due to its being serviced pursuant to this warranty. The terms of the foregoing warranty shall be null and void if the Equipment has been altered or repaired without specific written authorization of Seller, or if Equipment is operated under environmental conditions or circumstances other than those specifically described in Seller's product literature or instruction manual which accompany the Equipment. Seller shall not be liable for any expense of any nature whatsoever incurred by the original user without prior written consent of Seller.

Seller shall not be liable to Purchaser for any and all incidental or consequential damages for breach of either expressed or implied warranties. However, some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to Purchaser. All express and implied warranties shall terminate at the conclusion of the period set forth herein. Any card which is enclosed with the equipment will be used by Seller for survey purposes only.

If the Equipment is described as used, it is sold as is and where is. If the contract covers equipment not owned by Seller at this date, it is sold subject to Seller's acquisition of possession and title.

EXCEPT AS SET FORTH HEREIN, AND EXCEPT AS TO TITLE, THERE ARE NO WARRANTIES, OR ANY AFFIRMATIONS OF FACT OR PROMISES BY SELLER, WITH REFERENCE TO THE EQUIPMENT, OR TO MERCHANTABILITY, FITNESS FOR A PARTICULAR APPLICATION, SIGNAL COVERAGE, INFRINGEMENT, OR OTHERWISE, WHICH EXTEND BEYOND THE DESCRIPTION OF THE EQUIPMENT ON THE FACE HEREOF.

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